



## Wavelength tunable MEMS VCSELs

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# WAVELENGTH TUNABLE MEMS VCSELS



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DTU Fotonik

A thesis submitted in partial fulfillment for the degree of  
Doctor of Philosophy

Supervisors

Kresten Yvind  
Ole Hansen

Technical University of Denmark  
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## ABSTRACT

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MEMS VCSELs are one of the most promising swept source (SS) lasers for optical coherence tomography (OCT) and one of the best candidates for future integration with endoscopes, surgical probes and achieving an integrated OCT system. However, the current MEMS-based SS are solely based on the III-V material system, which is expensive and challenging to work with. Furthermore, the actuating part, i.e., MEMS, is on the top of the structure which brings a strong dependence on packaging to reduce its sensitivity to the operating environment. This thesis addresses these design drawbacks and proposes a novel design framework. The proposed device uses a high contrast grating mirror on a MEMS stage as the bottom mirror, all of which defined in an SOI wafer. The SOI wafer is then bonded to an InP III-V wafer with the desired active layers, thereby sealing the MEMS. Finally, the top mirror, a dielectric DBR (7 pairs of  $\text{TiO}_2$ - $\text{SiO}_2$ ), is deposited on top. A systematic study on the integration of InP to Si using a low-temperature bonding process with  $\text{Al}_2\text{O}_3$  as the intermediate layer is presented. The proposed device is based on a silicon substrate with MEMS defined on a silicon membrane in an enclosed cavity. Thus the device is much more robust than the existing MEMS VCSELs. This design also enables either a two-way actuation on the MEMS or a smaller optical cavity (pull-away design), i.e. wider FSR (Free Spectral Range) to increase the wavelength sweep. Fabrication of the proposed device is outlined and the results of device characterization are reported.

## RESUMÉ

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MEMS VCSELs er en af de mest lovende bølgelængdejusterbare (SS) lasere for optisk kohærens tomografi (OCT) og en af de bedste kandidater for fremtidig integration med endoskoper, kirurgiske sonder og realisering af et integreret OCT system. Sædvanlige MEMS-baserede SS er dog baseret på III-V materialesystemer, som er dyre og svære at arbejde med. Derudover, er den bevægelige del, dvs. MEMS, på toppen, hvilket forårsager en stærk afhængighed af pakningens evne til at reducere indflydelsen fra det operative miljø. Denne afhandling adresserer disse design ulemper og foreslår et nyt designkoncept. Den foreslåede enhed har et bundspejl bestående af et høj-kontrast-gitter på en MEMS platform fremstillet i en SOI skive. SOI skiven bindes kemisk til en InP III-V skive med de ønskede aktive lag, som dermed forsegler MEMS strukturen. Til sidst, bliver et dielektrisk DBR spejl (7 par  $\text{TiO}_2$ - $\text{SiO}_2$  lag) placeret på toppen. Et systematisk studie om integrationen af InP til Si ved lav-temperature kemiske bindingsprocesser med  $\text{Al}_2\text{O}_3$  som det midterste lag bliver ligeledes præsenteret. Den foreslåede enhed er baseret på et SOI substrat med MEMS udformet på en silicium membran i en lukket kavitet. Dermed er enheden langt mere robust end eksisterende MEMS VCSELs. Dette design muliggør derudover enten en tovejs bevægelse af MEMSen eller en kortere optisk kavitet for en bredere FSR (Free Spectral Range), som forøger bølgelængdejusterbarheden. Fabrikationen af det foreslåede design skitseres og resultaterne fra karakteriseringen af enheden rapporteres.

## PUBLICATIONS

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The following publications have been authored or coauthored during the course of the Ph.D. project.

### JOURNAL AND CONFERENCE ARTICLES

- Sahoo, H. K., Ansbæk T., Ottaviano, L., Semenova, E., Hansen, O., and Yvind, K., "Optically pumped 1550nm wavelength tunable MEMS VCSEL." Proceedings of SPIE . SPIE - International Society for Optical Engineering. 2016.
- Sahoo, H. K., Ansbæk T., Ottaviano, L., Semenova, E., Hansen, O., and Yvind, K., "1550nm optically pumped wavelength tunable MEMS VCSEL." European Semiconductor Laser Workshop . 2017.
- Sahoo, H. K., Ottaviano, L., Zheng, Y., Hansen, O., and Yvind, K., "Low temperature bonding of heterogeneous materials using Al<sub>2</sub>O<sub>3</sub> as an intermediate layer." Journal of Vacuum Science & Technology B, Vol 36, Issue 1, 011202. 2018.
- Sahoo, H. K., Ansbæk T., Ottaviano, L., Semenova, E., Hansen, O., and Yvind, K., "Wavelength tunable MEMS VCSELs for OCT Imaging." Vertical-Cavity Surface-Emitting Lasers XXII. International Society for Optics and Photonics, Vol. 10552. 2018.
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Demonstration of Photonic Crystal Laser with Buried Heterostructure". CLEO. 2017.

- Sakanas, A., Yu, Y., Semenova, E., Ottaviano, L., Sahoo, H. K., Mørk, J., and Yvind, K., "Photonic Crystal with Buried Heterostructure Platform for Laser Devices Directly Bonded to Si". Frontiers in Optics - Laser Science. 2017.
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- Zheng, Y., Pu, M., Sahoo, H. K., Semenova, E., and Yvind K., "High quality factor microring resonators in AlGaAs-on-sapphire". Applied Physics Letters. 2018. (To be submitted)

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## ACRONYMS

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ALD	atomic layer deposition
BCB	Benzocyclobutene
BW	bandwidth
CMOS	complementary metal oxide semiconductor
CPD	critical point drying
DBR	distributed Bragg reflector
DIW	deionized water
DRIE	deep reactive-ion etching
DTU	Technical University of Denmark
DUV	deep ultraviolet
FDML	Fourier domain mode locking
FEA	finite element analysis
FIB	focused ion beam
FP	fabry perot
FSR	free spectral range
FWHM	full width at half maximum
GaAs	galium arsenide
Ge	Germanium
HCG	high contrast grating
HF	hydrofluoric acid
HMDS	hexa-methyl-disilazane
IBSD	ion beam sputter deposition

ICP	inductively coupled plasma
IPA	isopropyl alcohol
InGaAlAs	indium gallium aluminium arsenide
InGaAsP	indium gallium arsenide phosphide
InGaAs	indium galium arsenide
InP	Indium Phosphide
KI	potassium iodide
LPCVD	low pressure chemical vapor deposition
MEMS	microelectromechanical systems
MOCVD	metalorganic vapour phase epitaxy
NIR	near-infrared
OCT	Optical coherence tomography
OSA	optical spectrum analyzer
PBSG	phosphorus boron silicate glass
PECVD	plasma-enhanced chemical vapor deposition
QD	quantum dot
QW	quantum well
RCA	standard cleaning steps developed at Radio Corporation of America
RIE	reactive-ion etching
SD-OCT	spectral domain - optical coherence tomography
SEM	scanning electron microscope
SLD	Superluminescent diode
SMSR	side mode suppression ratio
SNR	signal-to-noise ratio
SOA	semiconductor optical amplifier

SOI    silicon on insulator

SS-OCT    swept source - optical coherence tomography

SS    swept source

Si    Silicon

TD-OCT    time domain - optical coherence tomography

TEOS    tetraethyl orthosilicate

TMAH    tetramethylammonium hydroxide

TMA    trimethylaluminum

VCSEL    vertical-cavity surface-emitting laser

WDM    wavelength-division multiplexer

bHF    buffered hydrofluoric acid

## INTRODUCTION

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### 1.1 OPTICAL COHERENCE TOMOGRAPHY

Optical coherence tomography (OCT) is a non-invasive imaging technique which can be used to obtain high-resolution cross-section imaging. It is similar to ultrasound imaging, except it uses light instead of sound and uses backscattered light from the tissue to reconstruct the tissue structure. It is based on Michelson Interferometer system, shown in Figure 1.1. Light from a source is directed at a beam splitter which directs the light in two directions - one aimed at the sample and the other at a reference mirror. The reflection from the sample and the reference mirror are then interfered to obtain depth information of the sample.

OCT as a technology and research community has grown rapidly in a span of 26 years since its introduction in 1991. [29, 41] Imaging resolution and speed have increased 10 and 1 000 000 times respectively [29]. The application area which was initially eye imaging [41] has, now, expanded to cardiology,[12, 58, 90, 110] dermatology, [11, 17, 106] urology[94] etc. It has also been integrated into endoscopes [36, 57, 83, 95] and surgical probes [18] for providing physicians with real-time data. OCT has also been coupled with other imaging technologies such as multiphoton tomography, [51, 93, 109] non-linear microscopy [38, 105] and photoacoustic imaging,[48, 56, 111] to extract more enriched information. In order to continue this trend and extent to more application domains, OCT systems need to be simplified. The ultimate goal should be to integrate OCT on a chip, in a compact form factor.

OCT was first introduced by Huang et al. [41]. They used low coherence light as the source and the reference arm was continuously moved to interfere across the backscattered light on a photodetector. It was referred to as time domain - optical coherence tomography (TD-OCT). It was an important breakthrough enabling in-vivo



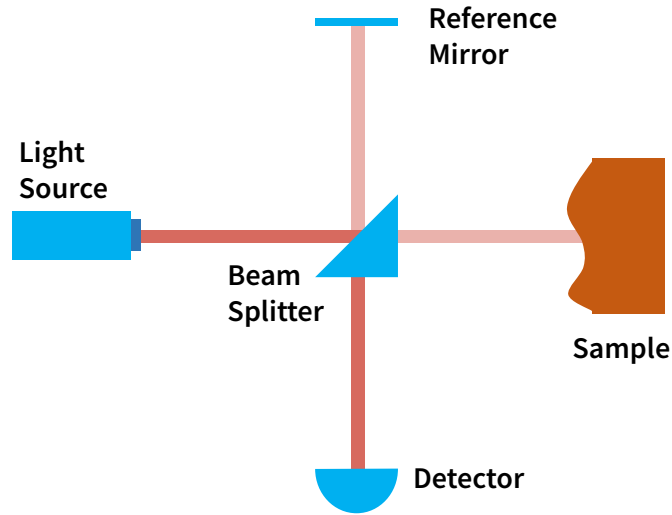


Figure 1.1: Illustration of a Michelson Interferometer setup.

imaging with much better resolution than ultrasound. However, it was noisy and was limited in the operation speed by the mechanically moving reference arm.

The light source used in TD-OCT was a broadband source and the backscattered light from the sample had information across the spectrum. So, a better way to decode the stored information is to look at the interference across the spectrum. Fixing the reference arm and replacing the photodetector with a spectrometer enabled this. Referred to as spectral domain - optical coherence tomography (SD-OCT), this was first reported by Fercher et al.[35]. SD-OCT is almost two orders of magnitude faster than TD-OCT. It is also better in resolution with a much-improved signal-to-noise ratio (SNR). This has fuelled a lot of interest in the field and SD-OCT is the most used OCT system in the industry today. The spectrometers used in SD-OCT, however, are quite expensive. The cost scales even up for longer wavelengths, where indium gallium arsenide (InGaAs) arrays are required. In addition, use of supercontinuum sources (which are also expensive) for wide broadband sources also result in noisy signals.

An alternate method is to perform frequency domain OCT using a tunable laser source instead of a broadband source and a photodetector instead of the spectrometer. It is much faster and has a better signal to noise ratio. It is termed as swept source - optical coherence tomography (SS-OCT) in view of sweeping the wavelength at the source. SS-OCT is relatively new and attractive because swept source (SS) light sources have the potential to achieve high scan speeds<sup>1</sup>, better resolution and deeper penetration at a relatively lower cost.[68][68]

**LIGHT SOURCE** Light sources sit at the core of the different types of OCT systems discussed in the previous section and hold the key to future high resolution, ultra-fast imaging systems. For TD-OCT and SD-OCT, an ideal light source should have a wide bandwidth with low noise and should have relatively flat power output across the entire spectrum. Bandwidth is particularly interesting as it is inversely proportional to the axial resolution. However, the ideal source is difficult to achieve. Superluminescent diode (SLD)s and supercontinuum sources are the two most used sources. SLDs are the current favourite with bandwidth in the order of 100-200 nm based on the wavelength of operation. Supercontinuum sources, on the other hand, provides an ultra-wide spectrum of ~2000 nm, but at the cost of high noise in the signal. A common approach has been to take the average of repeated measurements which is definitely not desirable from a speed perspective.

An ideal source for SS-OCT is a narrow linewidth laser sweeping at a high speed across a wide bandwidth. It is also desirable to maintain a uniform output power across the spectrum. There are many choices for SS technologies in the market, some of which are discussed in the next section. But, none of them has matured enough to replace the existing SD-OCT systems.

## 1.2 SWEPT SOURCES

SS-OCT technologies have already established themselves superior to SD-OCT and TD-OCT. They are much faster, have a better signal-to-noise ratio (SNR) and can image much deeper. However, the

---

<sup>1</sup> Scan in this thesis refers to A-scan, i.e. depth scanning.

technology space is still growing with new and better sources constantly being designed. Currently, they are more expensive than SD-OCT, but with a simpler design, it can be produced in a compact form and at a lower cost in the future. Here are some of the interesting SS technologies which have already been commercialized.

**FDML** Fourier domain mode locking (FDML) lasers [43, 44, 50, 107] are the fastest swept sources with A-scan speed as high as 5.2 MHz. They have also achieved a wideband tuning of 220 nm at 1300 nm with a power output of 100 mW. FDML lasers are known for providing a stable output with long coherence and low noise. Unfortunately, they are table-top fibre-based designs and are not easily scalable. Thus, in spite of the outstanding performance, FDML lasers have not gained traction.

**EXTERNAL CAVITY LASER** Axsun and Exalos are two companies working on two different external cavity laser systems. Axsun [67] uses an external cavity laser with a tunable microelectromechanical systems (MEMS) fabry perot (FP) filter as one of the mirrors and broadband semiconductor optical amplifier (SOA) as the gain, along with other optical components. It has demonstrated a tuning width of 140 nm at 1310 nm with an output of around 20 mW. Exalos [30] uses a similar setup to that of Axsun's. The MEMS FP filter is replaced with a MEMS scanning mirror, and a proprietary diffraction grating. It also delivers a very similar performance of 150 nm tuning at 1310 nm with a power output of 20 mW. The external cavity lasers are built using optical components and thus require a quite good alignment with temperature control for the desired performance. Furthermore, these are still macro-scale design with and scan speeds are limited to about 200 kHz after which the coherence drops quickly..

**AKINETIC** Insight akinetic SS [3, 16] are all semiconductor light sources with software controlled wavelength sweeping. It uses two sampled grating distributed Bragg reflector (DBR) mirrors along with cavity gain to define the laser cavity. Application of a desired current changes the refractive index of the elements which then changes lasing wavelength. It does not have any mechanical moving part, which makes it as one of the most reliable light sources.

It is however limited in its tuning range to around 80 nm at 1550 nm (with an output power of around 15 mW).

**MEMS VCSEL** microelectromechanical systems (MEMS) vertical-cavity surface-emitting lasers (VCSELs) are also semiconductor-based light sources and the most compact source of all (if no amplification is required). They have a very small footprint owing to the vertical cavity design. Generally, very highly reflective DBR mirrors along with III-V active material are used to define the cavity. Actuation of one of the mirrors contributes to the tunability. MEMS VCSELs from Praevium Research [46, 47] (commercialized by Thorlabs) are the current industry leader with high performing optically pumped SS lasers. They have demonstrated as wide as 150 nm tuning at 1310 nm [46] with scan speed as high as 1.2 MHz.

FDML lasers and MEMS VCSELs are the best SS lasers when it comes to performance. However, MEMS VCSELs are more future proof as it is already a wafer based technology and with improvements in design, it has the potential to deliver the required performance. An ideal SS should be able to operate at a speed of 200-400 kHz, with a tuning range of 100-150 nm with an almost flat output, low SNR and power output of  $> 10$  mW.[29] In addition, the technology should be cheap and robust. As Drexler et al. [29] point out, the perfect SS does not exist and the search continues. This thesis is an effort in that direction: to design the perfect SS - MEMS VCSEL for the OCT community.

### 1.3 MEMS VCSEL SS

Apart from the MEMS VCSEL design from Praevium Research, there are some noteworthy designs from Chase et al. [22], Gierl et al. [37] and OCTLight [7]. Unlike Praevium's design, these are electrically pumped devices. Figure 1.2 illustrates the design of the mentioned devices. The device from Praevium Research uses semiconductor DBR and dielectric DBR as the bottom and top mirrors respectively. The gain region is defined using III-V active material (quantum wells (QWs) in Indium Phosphide (InP)). The top mirror is actuated using electrostatics to achieve tuning. The device from Gierl et al. [37] is quite similar to Praevium's design, except the ac-

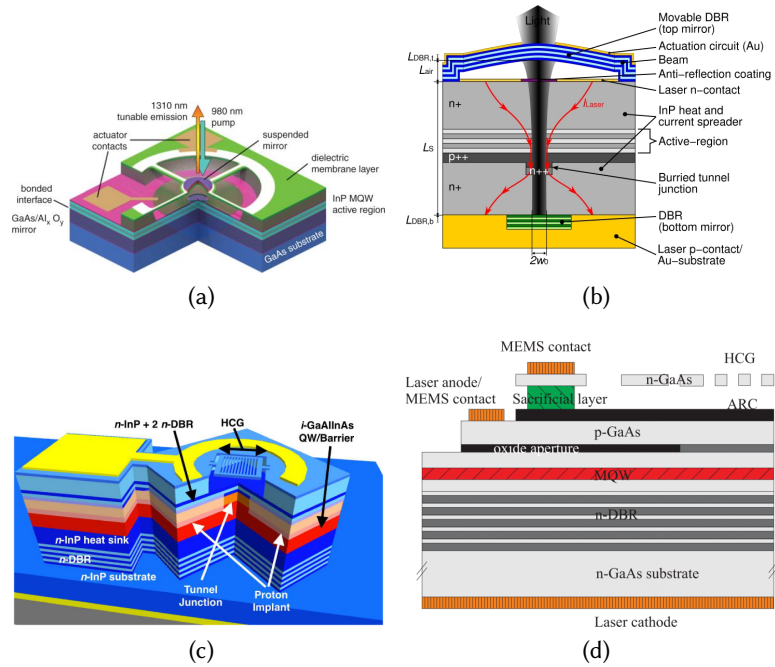


Figure 1.2: Device design of MEMS VCSELs from (a) Praevium Research [46] (b) Gierl et al. [37] (c) Chase et al. [22], and (d) OCTLight [7].

tuation mechanism being thermal. They use heating on already stressed dielectric membrane to actuate. The devices by Chase et al. [22] and Ansbæk et al. [7] are slightly different. They use a high contrast grating (HCG) mirror instead of a dielectric membrane, which are much more compact and can achieve very high reflectivity. They are also electrostatically actuated.

Overall, all the designs are based primarily on III-V material system, which is well known to be challenging to work with. In addition, the actuating part (MEMS) is on the top and is open to the working environment until packaged. Ideally, the MEMS/actuating part should be in a sealed cavity in order to have a good control of the mechanical dynamics. Else, any change in temperature and pressure may result in water condensation on the actuating electrodes which may lead to stiction, thereby ruining the device. Unfortunately, it is a feature in all the discussed MEMS VCSELs and is a

critical flaw. It needs to be corrected for SS to be more robust and reliable.

## 1.4 THESIS OUTLINE

MEMS VCSELSS are one of the promising candidates for the light source of the future OCT technologies. Advances in the integration of OCT on surgical probes and endoscopes require the sources to be more reliable and robust. The existing MEMS VCSEL designs are based on III-V (expensive and fragile) material systems and are sensitive to working environment (open MEMS) unless packaged. This PhD work addresses these drawbacks and proposes a novel MEMS VCSEL design. The proposed design deviates from the usual MEMS VCSEL design framework and takes a step closer to a more robust device. Ideally, the best solution is an electrically pumped version of the proposed device. However, this project is a step towards it. The device discussed in this thesis is optically pumped and establishes the foundation for the electrically pumped version. Furthermore, bonding of heterogeneous materials using low temperature (300 °C) is also discussed here. The integration method was crucial for realizing the device.

The thesis is broadly divided into three sections titled THE FOUNDATION, THE CRAFT and THE ACCOMPLISHMENT.

THE FOUNDATION includes Chapter 2 on theory and design of proposed MEMS VCSEL. The chapter discusses briefly on the theory of different elements of a MEMS VCSEL and dives into the simulation of the proposed device. It also covers the argument on how and why the proposed device is a big and much-needed leap in the design of MEMS VCSELS for more robust and reliable SS light sources. THE CRAFT encompasses the primary component of this PhD work - the realization of the proposed device. There are two chapters under this section. Chapter 3 covers a systematic study of integration method to bond III-V (InP) wafer with an silicon on insulator (SOI) wafer and Chapter 4 outlines an optimized fabrication process flow for the device. Some of the fabrication challenges are also discussed in this chapter. Finally, THE ACCOMPLISHMENT section looks at the characterization (in Chapter 5) of the device

and concludes this work with a short future outlook (in Chapter 6).

## Part I

### THE FOUNDATION





## THEORY AND DESIGN

---

This chapter aims at introducing a novel wavelength tunable micro-electromechanical systems (MEMS) vertical-cavity surface-emitting laser (VCSEL). The chapter begins with a brief introduction to VCSELs and tunability. The discussion is then directed towards the existing MEMS VCSEL design framework and how it can be modified to design a more robust MEMS VCSEL. The proposed MEMS VCSEL is then introduced and its advantages over the existing designs are presented. Next, the design and simulation of different elements of the proposed device are discussed. Finally, this chapter concludes with a review on the major roadblock to realizing the device.

### 2.1 VCSEL AND TUNABILITY

VCSELs are quite a common name in the data communication industry. They have established themselves as a standard for optical interconnects. By design, they have a vertical cavity and also emit light vertically. So, they need small estate on the wafer and can be mass fabricated on a wafer scale with on-chip testing possible during its fabrication cycle. This has primarily been the reason behind its wide acceptance.

#### 2.1.1 *Design*

VCSEL design is based on a fabry perot (FP) laser cavity as shown in Figure 2.1. The essential components for a VCSEL are two mirrors (with certain intensity reflectivities,  $R_t$  and  $R_b$ ) trapping the light and an active region providing gain,  $g$ . The distance between the mirrors defines the cavity length,  $L$ . Given a uniform medium with

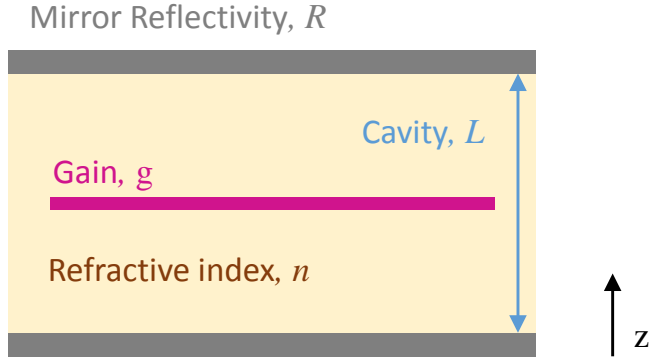


Figure 2.1: Illustration of a Fabry-Perot cavity with a gain medium.

a refractive index,  $n$ , between the 2 mirrors, the emission wavelength,  $\lambda$ , is given by

$$2nL = m\lambda \quad (2.1)$$

where  $m$  is a positive integer. Vertical cavity design means it has lower gain and power output compared to ridge lasers. At the same time, the small modal volume helps VCSEL in being more energy efficient and possibly having a lower lasing threshold.

**MIRROR** The cavity length for VCSELs is generally in the order of the wavelength range, which means the standing waves, between the mirrors, see a very short gain region. So, it is important not to lose a lot of light at the mirrors. The mirrors are, thus, designed to have high reflectivities to reduce the reflection losses at the ends. It is equally important to consider the reflectivity bandwidth (BW) of the mirrors and the relative difference in reflectivity between the mirrors for achieving a wide tuning band and lasing direction respectively.

**ACTIVE REGION** The gain in the active region of a VCSEL is provided by either quantum wells (QWs) or quantum dot (QD)s, which are either based on Indium Phosphide (InP) or gallium arsenide (GaAs) depending on the wavelength of interest. The band structure can be engineered to the desired emission wavelength.

An individual QW thickness is normally around 10 nm, which implies their position within laser cavity is critical for maximizing the effective gain,  $g_{eff}$  as seen by the standing wave  $E(z)$ .

$$g_{eff} = \Gamma g, \quad (2.2)$$

$$\Gamma = \frac{L}{d_a} \frac{\int_{d_a} |E(z)|^2 dz}{\int_L |E(z)|^2 dz}, \quad (2.3)$$

where  $\Gamma$  is the confinement factor defined by the overlap of the standing wave with the active layer and  $d_a$  is the thickness of the QW. [25, 65] In most cases, multiple QWs are grown centred at the field maximum to achieve the highest  $\Gamma$ . Next, in order to lase, the total gain of the system should be higher than the losses. The gain which is just equal to the losses is referred to as the gain threshold,  $g_{th}$ . It is the sum of the losses due to absorption and scattering in the medium (both active and passive),  $\alpha$  and the reflection losses at the mirrors.

$$g_{th} = \frac{1}{\Gamma} \left\{ \alpha + \frac{1}{2L} \ln \left( \frac{1}{\sqrt{R_t R_b}} \right) \right\}. \quad (2.4)$$

So, to summarize, an ideal VCSEL is a resonant cavity defined by highly reflective mirrors and high quality grown III-V active material with low scattering loss optimally placed for high confinement factor.

### 2.1.2 Adding tunability

Wavelength tunability can be achieved either by thermally heating a VCSEL [19, 33] or by physical movement of one of the mirrors.[7, 20, 37, 47] The former is usually slow and limited to few nm in range. The latter is more common and can help achieve much wider tuning. Only the latter case is considered in this study.

When one of the mirrors of a FP cavity is displaced relative to the other, the standing wave field inside the cavity changes accordingly (Figure 2.2). This, in turn, changes the emission wavelength. However the wavelength should be within the gain BW of the active region (Figure 2.3). Else, the losses in the cavity will be dominant

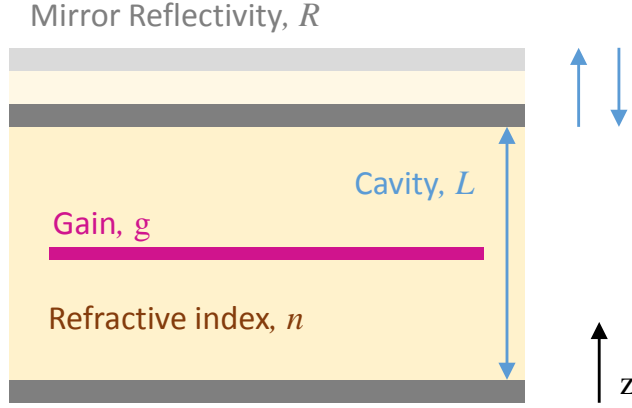


Figure 2.2: Illustration of a tuned Fabry-Perot cavity.

and lasing will not occur. The lasing mode is defined by the cavity length by Equation 2.1 and the free spectral range (FSR),  $\Delta\lambda$  is given by

$$\Delta\lambda = \frac{\lambda^2}{2nL} \quad (2.5)$$

A wider FSR is desirable for a wide tuning range without mode hopping. VCSELs have a small vertical cavity and hence a wide FSR. However, in an attempt to add tunability to the cavity, the mode hopping free tuning range may be reduced. The tunability may also be limited either by the gain BW or limits on the tuning mechanism. Further, the losses in the system are not necessarily constant across the wavelength spectrum as shown in Figure 2.3, which can be a due to the design of mirror reflectivity spectra. Again, the design and placement of QWs in the active region may also contribute to losses due to defects and low confinement respectively.

## 2.2 DESIGN

There are a number of existing MEMS VCSEL designs [6, 22, 37, 46, 82]. However, they are all based on a similar design framework. They borrow the design structure from a VCSEL design which is heavily dependent on III-V growth, which is a challenging job. VCSELs, from a design aspect, are multilayered structures with no moving

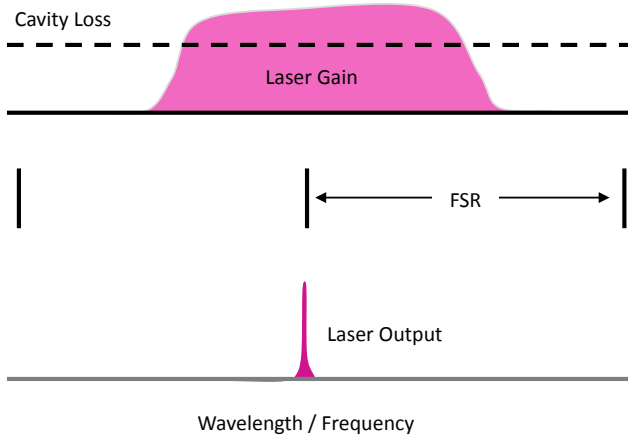


Figure 2.3: Gain and loss spectra, mode location and laser output.

part. Unlike VCSELS, MEMS VCSELS have a characteristic air-gap which is tuned using a movable mirror. The air-gap is a part of the optical cavity and contributes to the MEMS dynamics. So, it needs to be a controlled environment. There is also the chance of damaging the MEMS element from water condensation. These primary issues are addressed here and a new design system is proposed.

### 2.2.1 *Traditional Approach*

Figure 2.4 shows the design evolution of the MEMS VCSEL design from VCSELS. The bottom mirror in most cases is a grown low index contrast distributed Bragg reflector (DBR) mirror (or an oxidized DBR mirror[46]) on top a III-V substrate. The gain material is either grown along with the bottom mirror or bonded to the bottom mirror. As the bottom mirror sits on the top of the substrate, it is mostly the top mirror, which is actuated. It has been modified in some cases to be a dielectric DBR mirror stack or a high contrast grating (HCG) mirror. Both of them are huge improvements in terms of the resulting mirror thickness. The latter being the best. The challenge here is to achieve a very high reflectivity in the order of 99.9% as mentioned earlier. The dielectric DBR does a good job owing to the higher contrast difference than the III-V counter-

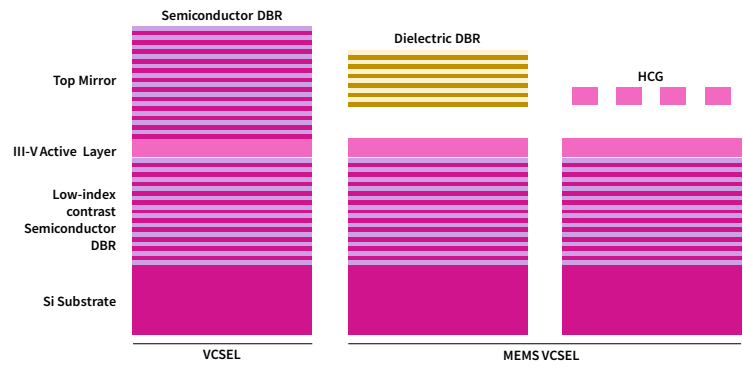


Figure 2.4: Illustration comparing the design framework of VCSELs and existing MEMS VCSELs.

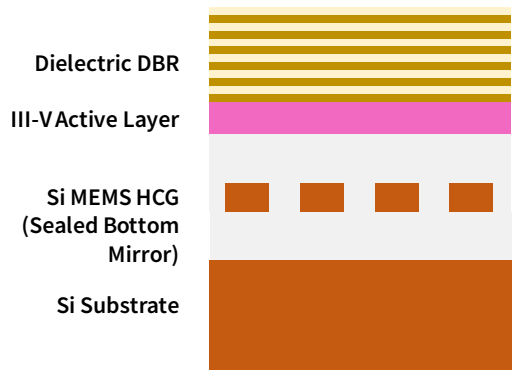


Figure 2.5: Sketch of the proposed MEMS VCSEL.

part. HCG has a very high reflectivity owing to the near wavelength thickness with high contrast grating structure. More on HCG is discussed later. Nevertheless, the actuating part is still the top mirror based on dielectric or III-V material.

2.2.2 *Make it Better*

The devices from Praevium research [46] and Chase et al. [22] are well designed MEMS VCSELs with great performance. In particular, use of dielectrics and HCG as mirrors helps in achieving a compact device. So, the design elements for mirrors have expanded to III-

V DBR, dielectric DBR and HCG, which inherently does not need to be III-V. The active region, on the other hand, will remain dependent on the III-V material system, primarily due to the ability to engineer the desired band structure and achieve high gain.

The proposed device needs to address two main issues: heavy dependence on III-V materials and the open actuation element. III-V materials are expensive, fragile and quite challenging to work with. The best alternative is the more established Silicon (Si) platform. There is a lot of established knowledge on Si processing and the Si substrates are cheaper and mechanically more robust to work with. Furthermore, it will open up possibilities for integration with Si photonics. With a Si substrate, the options for the bottom mirror are dielectric DBR and HCG. Defining a HCG on a Si layer of a SOI substrate and actuating it, addresses the second issue too. So, HCG is the perfect choice for bottom mirror. The active material still stays and the top mirror can be defined by a dielectric DBR. A sketch of the re-designed MEMS VCSEL is shown in Figure 2.5. To summarize, the proposed device is a Si substrate based MEMS VCSEL defined by a HCG mirror as the bottom mirror and dielectric DBR as the top mirror, and the actuating part is defined on Si which sits in a sealed cavity.

### 2.2.3 *Advantages from the Design*

The proposed design offers many advantages in comparison to the traditional approach. First and foremost, it is a huge step towards the more established and standard silicon platform. Apart from the gain material, everything is a standard complementary metal oxide semiconductor (CMOS) material. Encapsulating the actuating part (HCG on a MEMS frame) is another big plus. It gives a designer the ability to have a good control on the operating atmosphere of the MEMS - nitrogen or vacuum or other gas with the desired damping. Furthermore, the actuating part is now defined on Si, which is a much better material than its III-V counterparts in terms of robustness and reliability.

Apart from the very obvious benefits, the design brings a modular approach to the design of MEMS VCSELs, possibility to sweep in



2 directions and achieving a smaller cavity, without being limited by MEMS pull-in constraints.

**MODULAR DESIGN APPROACH** Unlike the traditional approach, all the elements can be designed and fabricated independently of each other. So, the design can be modified quite fast to accommodate any change in emission wavelength based on the application area.

The HCG, defined on SOI, can be modified to achieve wide band reflectivity close to 100 % over the desired wavelength range. The thickness of DBR layers and number of pairs can similarly be adapted to get the desired reflectivity spectrum. The active material which is grown independently can also be changed in accordance with the wavelength. Lastly, the air-gap which constitutes the major part of the optical path can also be adjusted on-the-go to have the desired cavity length. Summing up, all the elements in the design can be easily modified to realize tunable MEMS VCSEL for the desired wavelength. This is crucial when using MEMS VCSELs for applications in different wavelength regimes.

**BI-DIRECTIONAL TUNING** Another interesting aspect of the device is its ability to tune in two directions. The MEMS can be actuated by applying a voltage between the Si-layer of the SOI and either the Si substrate or the InP layer on the top. This is particularly important to increase the tuning range, which is limited to 1/3rd of the distance between the electrodes for electrostatic actuation. This limitation still holds good for the proposed device but the possibility to tune in two directions extends the limitation on tuning range to 1/3 of the total air gap (top and bottom of the MEMS).

**SMALLER CAVITY** The above mentioned constraint on electrostatic actuation distance has also been a bottleneck in designing MEMS VCSEL with a smaller cavity. Tunable air gap (between the actuating electrodes) is a part of the optical path and reducing it will result in reducing the available tuning range. In the proposed design, to achieve a smaller cavity, the top air-gap can be reduced and only bottom air-gap is tuned. In other words, the proposed design adds a pull-away actuation unlike the existing devices.

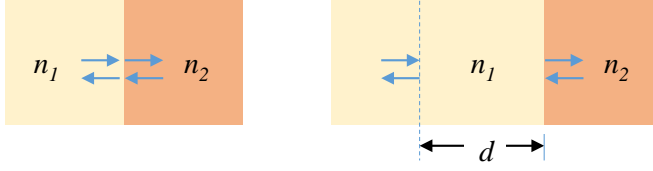


Figure 2.6: (Left) Interface between 2 materials with refractive index  $n_1$  and  $n_2$ . (Right) Homogeneous material with a thickness,  $d$ , followed by an interface. Adapted from [85].

## 2.3 SIMULATIONS

Simulation of the mirrors and the device as a whole was an important step in realizing the device. Design and simulation of dielectric DBR, HCG and the complete device are presented in this section. Important fabrication parameters for the device fabrication are obtained from the simulations.

The proposed device can either be designed for electrical pumping or optical pumping. An electrical version will need a study on tunnel junctions for current injection. An optical version is much simpler. Thus, the latter was considered for this thesis. Thermal lensing is used in this study for mode definition while optical pumping the device. So, the thermal properties of the device and optical mode definition are also discussed.

The wavelength for the device was chosen to be 1550 nm. The choice was influenced by the availability of grown 1550 nm active layer on top of the drive to realize the device. Ideally, the wavelength for the device should be decided based on the application requirements. Again, the modular design frame of the proposed device should enable easy adaption to the desired wavelength.

### 2.3.1 Dielectric DBR Mirror

The DBR is a mirror structure defined using alternating layers of high and low refractive index materials. The fundamental principle of reflection and transmission at the interface of two differ-

ent materials forms the underlying basis for the mechanism. For normal incidence of light at a interface defined by two materials with refractive index  $n_1$  and  $n_2$  (Figure 2.6 (Left)), the reflectance amplitude,  $r_{12}$ , and transmittance,  $t_{21}$ , are given by Fresnel equations.

$$r_{12} = \frac{n_1 - n_2}{n_1 + n_2}, \quad (2.6)$$

$$t_{21} = \sqrt{(1 - |r_{12}|^2)} = \frac{2n_2}{n_1 + n_2} \quad (2.7)$$

Similarly,  $r_{21}$  and  $t_{12}$  can be determined to define S matrix formalism for the interface between the two materials.

$$\begin{bmatrix} t_{12} & r_{21} \\ r_{12} & t_{21} \end{bmatrix} = \frac{1}{n_1 + n_2} \begin{bmatrix} 2n_1 & n_2 - n_1 \\ n_1 - n_2 & 2n_2 \end{bmatrix} \quad (2.8)$$

where the subscript  $ij$  represents the direction of light. and it can also be converted to M matrix form as

$$M = \frac{1}{2n_2} \begin{bmatrix} n_2 + n_1 & n_2 - n_1 \\ n_2 - n_1 & n_2 + n_1 \end{bmatrix} \quad (2.9)$$

When a layer has a defined thickness  $d$ , (Figure 2.6 (Right)) the above matrix can be modified to take into account phase. [85]

$$M = \frac{1}{2n_2} \begin{bmatrix} (n_2 + n_1)e^{-jn_1k_0d} & (n_2 - n_1)e^{jn_1k_0d} \\ (n_2 - n_1)e^{-jn_1k_0d} & (n_2 + n_1)e^{jn_1k_0d} \end{bmatrix}, \quad k_0 = 2\pi/\lambda \quad (2.10)$$

For, multiple layers the  $M$  matrices can be multiplied to define a combined transfer matrix  $M$  for a DBR stack. When the optical thickness of each layer is equal to  $\lambda/4$ , the reflected light goes through constructive interference and thus behave as a mirror. For a stack of  $N$  pairs of alternating layers of material (thickness of each layer is equal to  $\lambda/4n_i$ ) with refractive indices  $n_1$  and  $n_2$ , the reflection  $R_N$  achieved is given by [64, 85, 88]

$$R_N = \left[ \frac{n_2^{2N} - n_1^{2N}}{n_2^{2N} + n_1^{2N}} \right]^2 \quad (2.11)$$

The larger the number of such pairs ( $N$ ), the stronger is the reflection. The index contrast is equally important. It contributes both to the reflection intensity and BW. This is primarily the reason

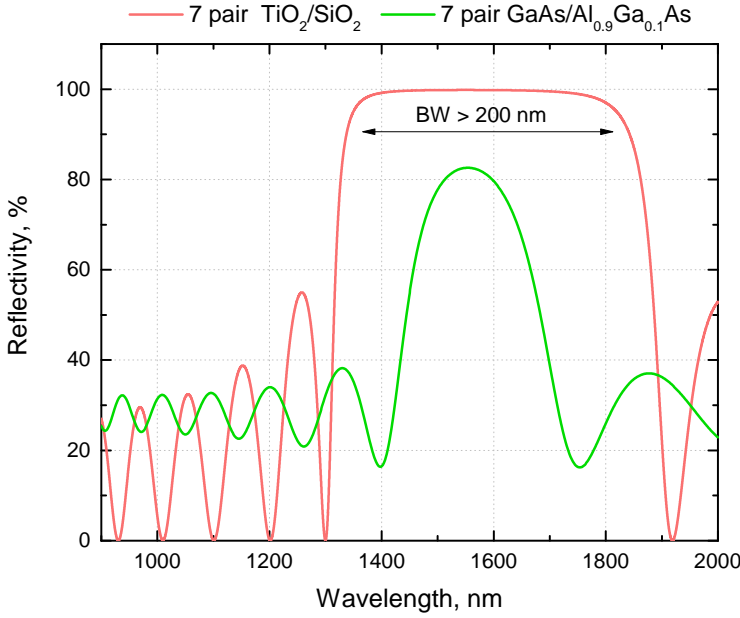


Figure 2.7: Reflectivity plot for a dielectric DBR (  $\text{TiO}_2/\text{SiO}_2$ ) compared with a semiconductor DBR ( $\text{GaAs}/\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ ).

behind dielectric DBRs gaining more attention in VCSEL design than the semiconductor DBRs. Figure 2.7 shows the reflectivity plot for dielectric DBR stack using  $\text{TiO}_2$  (2.31) and  $\text{SiO}_2$  (1.44) as the alternating materials. Each of the layer is quarter of the design wavelength (1500 nm) thick. Compared to a  $\text{GaAs}$  (3.37) /  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$  (2.95) semiconductor DBR stack, the dielectric mirror provides much higher reflectivity with a wider BW, for the same number of pairs. Even with a larger number of pairs, a semiconductor DBR will have a narrower BW than a dielectric DBR.

The proposed device will be optically pumped. So, for an efficient pumping, the pump wavelength must pass through the top mirror in order to reach the active region. The most common pump wavelengths in use are 980 nm and 1310 nm laser sources. The dielectric DBR was, thus, designed to have minimal reflections at these wavelengths. In order to achieve this, the DBR was defined using propagation matrices across the layers to calculate the reflectance [6, 69] and the individual layer thicknesses were varied to minimize the following parameter, which is a sum of the reflection at

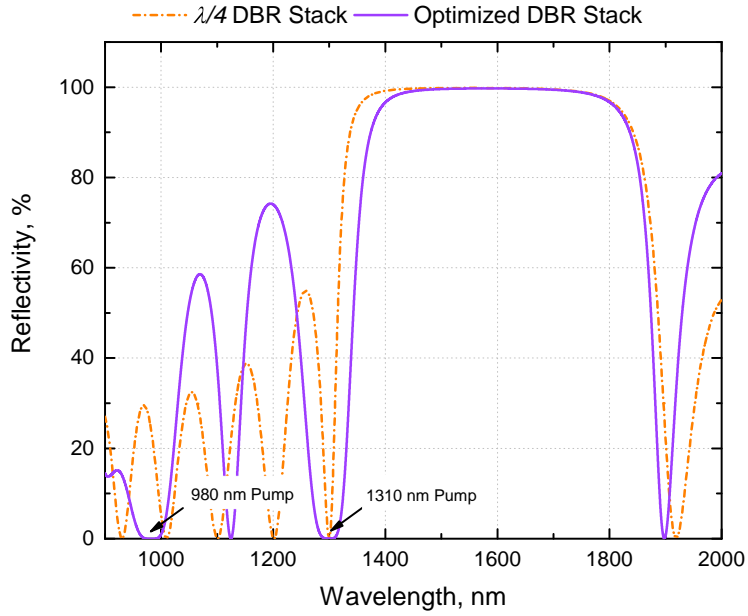


Figure 2.8: The reflectivity plot of 7 pair of  $\text{TiO}_2$  and  $\text{SiO}_2$ . The plot shows the comparison of reflectivity for a standard DBR with quarter wavelength thickness against an optimized DBR stack.

980nm,  $R_{980\text{nm}}$  and 1310nm,  $R_{1310\text{nm}}$ , and transmission at 1550nm,  $1 - R_{1550\text{nm}}$ .

$$R_{980\text{nm}} + R_{1310\text{nm}} + (1 - R_{1550\text{nm}})$$

Figure 2.8 shows the resulting spectrum and the corresponding optimized stack can be found in A.26. It now retains a high reflectivity around the desired lasing wavelength and a low reflectivity around the possible pump wavelengths. For an electrical version of the proposed device, the above optimization for pump wavelength is not a requirement. However, it is a useful feature for optically testing the fabricated sample, without having to adjust the electrical probes.

### 2.3.2 HCG Mirror

A HCG is used as the bottom mirror for the proposed MEMS VCSEL. was first reported by Mateus et. al.[62] and it has been imple-

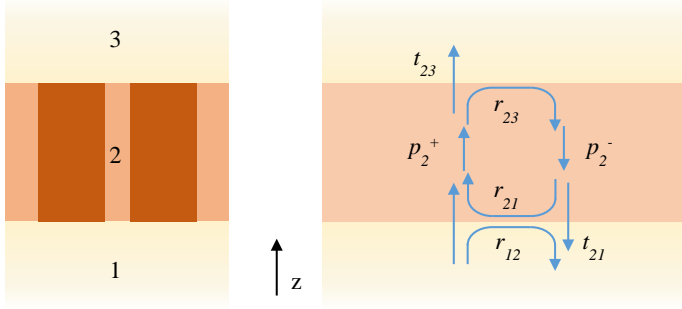


Figure 2.9: (Left) Illustration of the geometry used for modeling HCG. (Right) Reflectivity and transmission at the interfaces of the structure. Adapted from [53].

mented as a mirror for a wide range of devices. [6, 21, 34, 39, 42, 92, 112] The dimensions of the HCG can be tuned to achieve a desired reflectivity spectrum. Additionally, it is defined on a single high index material layer, which makes it easy to fabricate in contrast to the multilayer DBRs. Owing to its light weight, the mirror is an excellent choice for mechanical actuation.

For this thesis, the HCG was modeled using the Modal Method [53]. The structure was divided into layers of uniform permittivity along the propagation direction (z-axis). It is acceptable to have a variation in the lateral direction as long as the permittivity remains constant in the z-axis. The structure for HCG simulation was defined as shown in Figure 2.9. In the Modal Method, first, eigenmodes are determined for each individual layer using Fourier expansion of plane waves in the transverse direction. The electric and magnetic fields in the layers are then defined in terms of those eigenmodes. The tangential component of the fields should be continuous at the layer interfaces. This was used to determine the reflection and transmission at the boundaries of the structures. For a 3-layer system like ours, the reflectivity of the HCG is a summation of the reflection at the interface between layer 1 (low-index) & layer 2 and the transmitted component of the light trapped in the layer 2. Using scattering matrix formalism, the total reflectivity of the HCG,  $r_{13}$ , can be represented by[53]

$$r_{13} = r_{12} + t_{21} p_2^- r_{23} p_2^+ (I - r_{21} p_2^- r_{23} p_2^+)^{-1} t_{12} \quad (2.12)$$

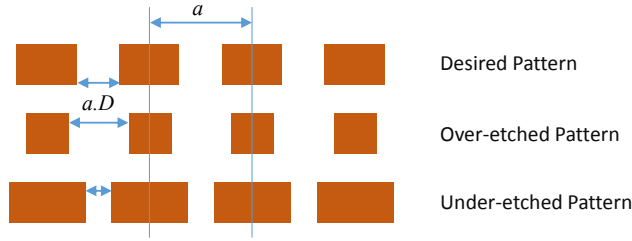


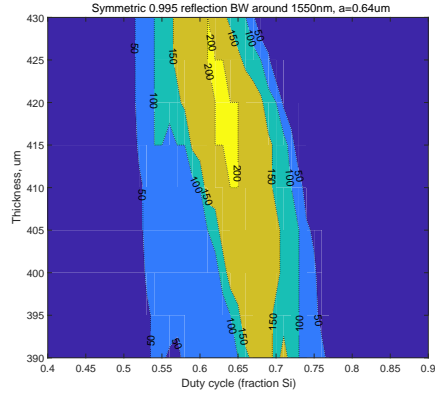
Figure 2.10: Illustration showing the dependence of HCG period,  $a$ , and duty cycle,  $D$ , dependence on pattern transfer and etching.

where  $r_{ij}$  indicates the reflection in layer  $i$  w.r.t layer  $j$ ,  $t_{ij}$  represents the transmission from layer  $i$  to  $j$  and  $p$  is propagation in the medium.  $(I - x)$ , where  $I$  is the identity matrix, is used to represent infinite round trips in the layer 2. CAMFR [13] was used to simulate the HCG structure.

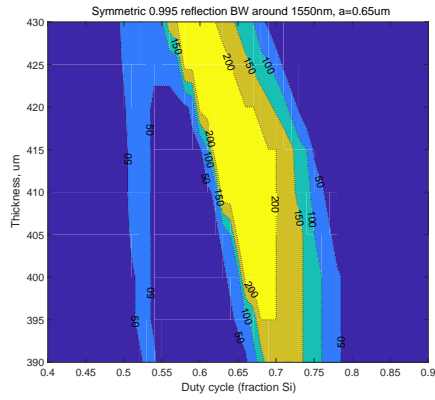
The reflectance of a HCG is primarily dependent on 3 parameters: periodicity of the alternating high and low index material (Si and air in our case) represented by thickness of the layer,  $t$ , period,  $a$ , and duty cycle,  $D$ , of the grating. Previous experience [6] helped narrow down the parameter space to  $390 \text{ nm} < t < 430 \text{ nm}$ ,  $560 \text{ nm} < a < 750 \text{ nm}$  and  $0.41 < D < 0.9$ . HCG will be defined on the Si layer of SOI. So, it was important to have the Si layer thickness close to that of the available wafers from SOI suppliers. The duty cycle of the grating will be defined by a dry etch process. So, there might be small variations due to processing parameters. The period stays unaffected by the fabrication variations as explained in Figure 2.10.

The primary aim for the HCG simulations was to determine the parameters for achieving high reflectivity (99.5 %) over a broad spectrum ( $\sim 100\text{-}150 \text{ nm}$ ) and tolerances of those parameters. As mentioned above, period of the grating is a more robust parameter than the other two. So, the reflectivity variation w.r.t  $t$  and  $D$  are plotted for various  $a$  (Figure 2.11). Having a period of 650 nm promises a high reflectivity of 99.5 % with around 200 nm BW and good tolerance range for  $t$  and  $D$ .

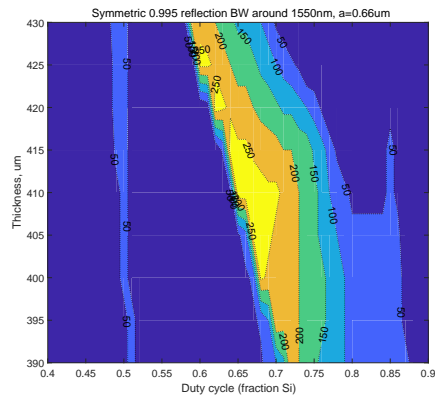
A HCG mirror defined on a Si layer with  $t$  equal to 410 nm,  $0.65 < D < 0.69$ , and  $a$  equal to 650 nm will give a high reflectivity of 99.5



(a)



(b)



(c)

Figure 2.11: Reflectivity of 99.5% with contour of BW centered around 1550 nm plotted for different HCG thickness,  $t$ , duty cycle,  $D$ , and period,  $a$  = (a) 640 nm (b) 650 nm (c) 660 nm.



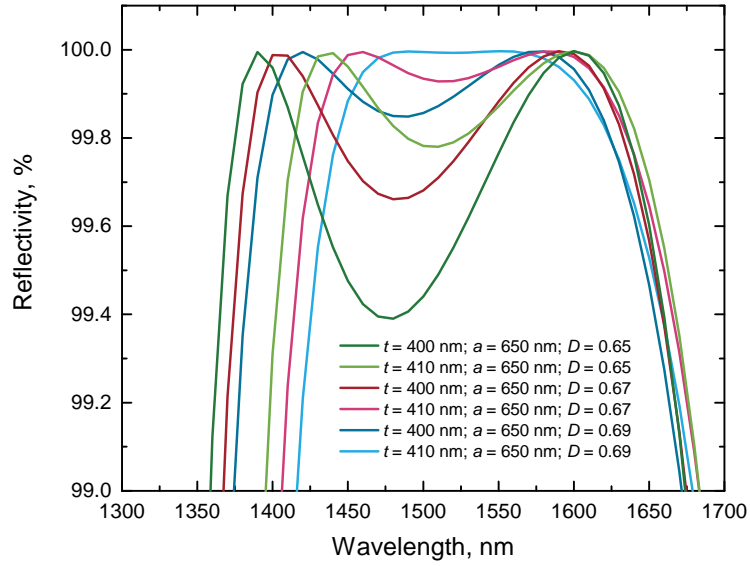


Figure 2.12: Reflectivity plotted against wavelength for various HCG parameters.

% with BW of 200 nm around 1550 nm. Figure 2.12 shows the reflectivity plot for the above mentioned parameter space. It can be seen that a very high reflectivity with a wide BW is maintained over a range of parameters. This is what makes HCG as a robust design element from a fabrication point of view.

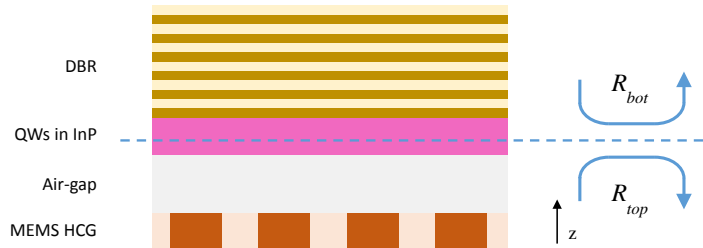


Figure 2.13: Illustration of the device model used in the simulation.

### 2.3.3 Device Simulation

The complete device was also modeled using modal method in CAMFR [13, 14]. The MEMS VCSEL structure was divided into two parts. (Figure 2.13) The top part includes part of InP with QW structure and dielectric DBR mirror, with a reflection  $R_{top}$  as seen from the bottom. Similarly, the bottom part comprises of the remaining InP, air gap, and HCG MEMS mirror, with a reflection of  $R_{bot}$ , seen from the top. The lasing mode was found by satisfying the condition of unity round trip gain for the cavity. Considering the losses in the material, the mirror loss and the gain material overlap with the electric field, an effective gain (threshold gain) was determined which will ensure unity round-trip gain. This information along with the gain of the grown QWs can be used to determine an approximate gain BW for the device. Another objective of the simulation was to look at the lasing wavelength as the gap was changed. Figure 2.14 shows the refractive index profile of the defined structure overlapped on the resulting electric field. The alternating layers of  $\text{SiO}_2$  and  $\text{TiO}_2$  represent the top mirror, followed by a layer of InP with QW structures embedded in them, tunable airgap and HCG mirror. The air-gap was varied to simulate the tuning effect. For each air-gap, the corresponding cavity mode and threshold gain were determined. The reflectivity of both the mirrors, which varies as a function of the wavelength was also taken into consideration during the simulation. The tuned lasing wavelength corresponding to variation of air-gap is shown in Figure 2.15. Figure 2.16 shows a zoomed in view of the field around the QW structures (highlighted in yellow). The placement of the QWs close to the anti-node is essential to achieve a low threshold for the desired range. This information was used for the growth of QWs during fabrication.

This simulation data is valid for any zero (un-actuated) position of HCG. So, it can be used for both bi-directional tuning or small cavity design (Section 2.2.3). At the same time, care should be taken to ensure that the actuation regime (i.e. tuned wavelength region) is centered around the region with low threshold gain.

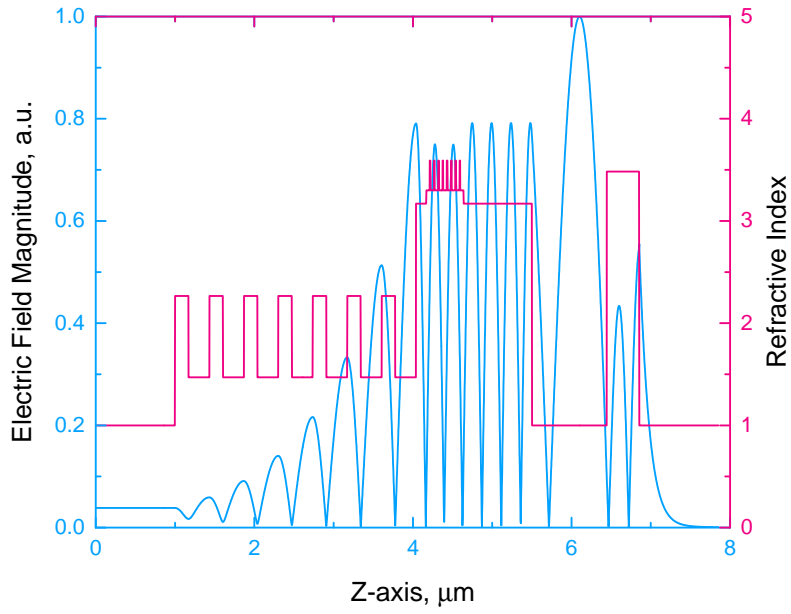


Figure 2.14: Electric field plotted on top of the device structure defined by the refractive index of the layers.

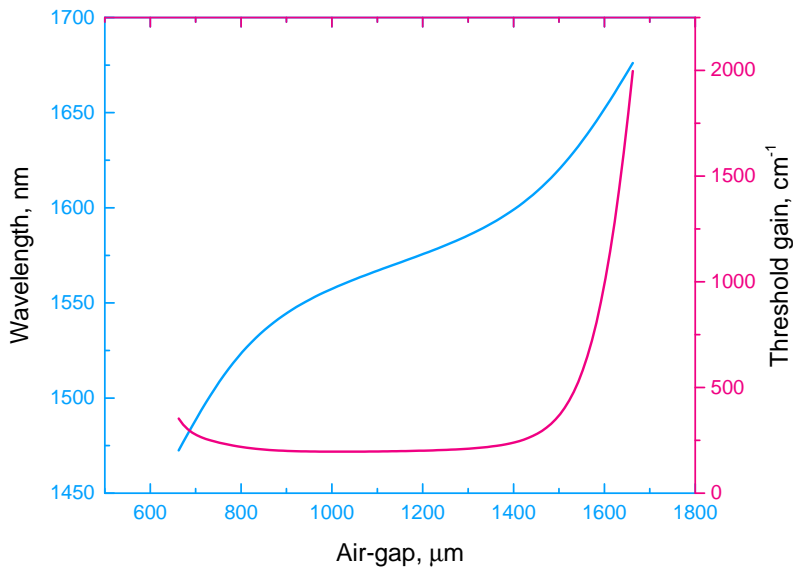


Figure 2.15: The lasing wavelength plotted against the corresponding air-gap (tunable component of the cavity length).

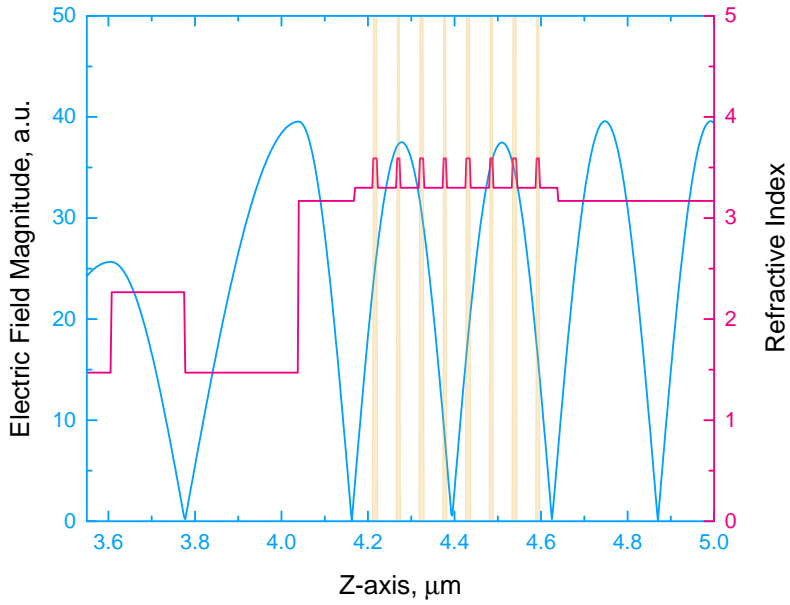


Figure 2.16: A zoomed-in image of Figure 2.14 showing the overlap of the field and the QWs. The QWs position is highlighted by yellow stripes. The placement is crucial to increase the confinement factor and decrease the threshold gain for lasing.

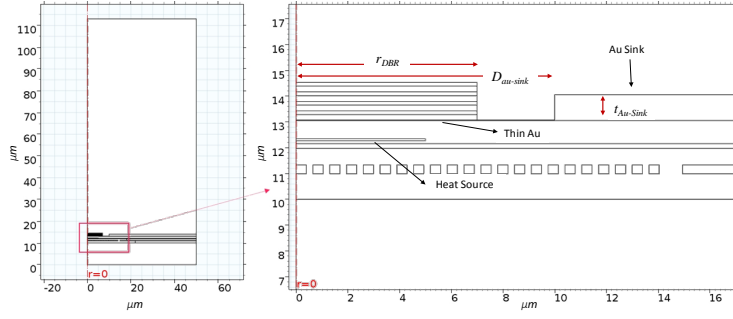


Figure 2.17: Illustration of the axis-symmetric model used for COMSOL thermal simulation.

### 2.3.4 Thermal Simulation

The proposed design uses thermal lensing as a part of lasing mode definition. When a pump beam is focused on the device, a certain part of the energy is absorbed by the active material. A part of that energy is spent for generation of photons and the rest is released as heat. The heat, in turn, results in the change in refractive index of the medium. The change in refractive index assumes a profile based on the pump spot, which then acts as a guide for the lasing mode. This is referred to as thermal lensing.

finite element analysis (FEA) on COMSOL was used to simulate thermal lensing on the proposed device. It was divided into two parts. The device was first modelled with a heat source in the active region which gave the radial temperature distribution of the device. This information was then used in another model to look at the possible optical modes for the corresponding refractive index profile. An analysis of heat transfer of the VCSEL was also performed to get information on the core temperature during lasing operation.

**TEMPERATURE PROFILE** An axis symmetric model was used for the simulation of temperature profile and heat transfer across the device. Figure 2.17 shows the model of the device. The device design in the model is quite similar to the device discussion. A heat source,  $Q$ , was defined in a rectangular region, positioned within the active material. A gold layer with a thickness,  $t_{Au-sink}$ , placed

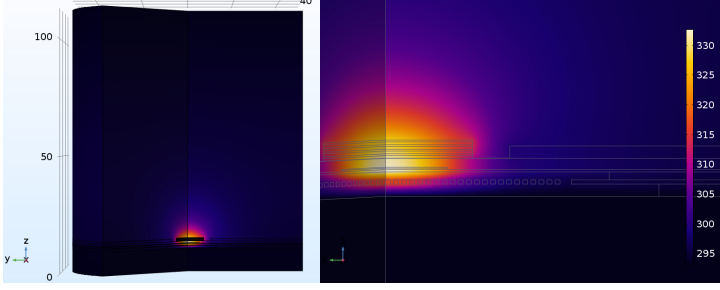


Figure 2.18: Temperature profile of the device due to heating caused from optical pumping.

at a distance,  $D_{Au-Sink}$  from the centre, was used as the heat sink. Also, in an attempt to be close to the heat source, a thin-Au layer (20 nm) extending from the centre to the thicker Au sink, was also considered.

The heat generated in the device is dependent on the pumping wavelength and spatial distribution of the pump beam. Based on the absorption, the pump power will also decay as it goes deeper into the device. For simplicity, the absorption was assumed to occur only in the rectangular heat source region, with a Gaussian profile[108] defined by

$$Q = \alpha I e^{-\alpha(z_0 + t_{heat} - z)} e^{-\left(\frac{r}{a}\right)^2}, \quad I = \frac{(1 - R)P}{\pi a^2} \quad (2.13)$$

where  $\alpha$  is the absorption coefficient of the incident laser in the active material,  $R$  is the reflection co-efficient,  $a$  is  $1/e$  radius of the pump beam,  $P$  is the total incident power,  $t_{heat}$  is the thickness of the active region and  $z_0$  is the bottom corner of the heat region in the model. For the simulation, 400 mW power was incident on the device with a  $\alpha$  of  $10^4 \text{ cm}^{-1}$ ,  $R$  of 0.3 with a beam size defined by  $a$  equal to  $6 \mu\text{m}$ . The top ( $\sim 100 \mu\text{m}$  away from the top in air) and the bottom (Si Substrate) of the simulation domain were kept at 293 K. The simulated temperature profile on the device is shown in Figure 2.18 and the heat flux in the radial direction is shown in Figure 2.19. Almost all of the heat was transferred from the centre in the lateral direction through InP. The InP layer with relatively higher thermal conductivity than that of the adjacent oxide layers is the preferred medium for heat transfer. And as soon as the heat sees the Au layer, It switches to the latter.

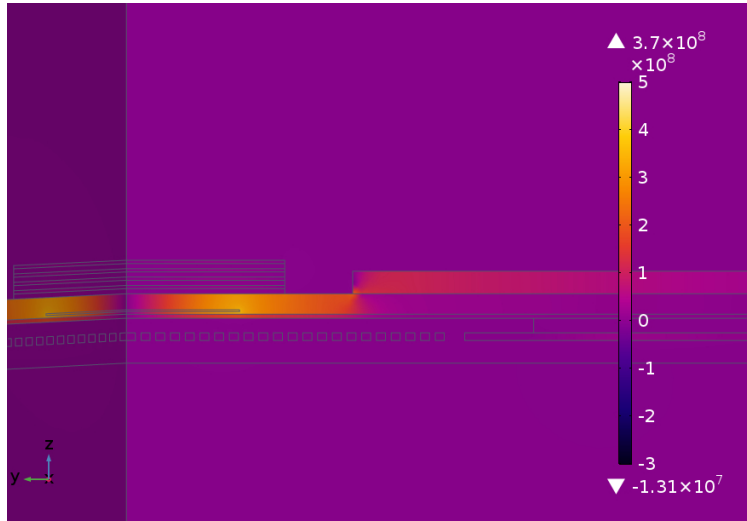


Figure 2.19: Radial component of the heat flux showing the heat transfer. The heat moves into the metal as soon as it sees it.

The presence of heat sink has a great impact on the core temperature. Au with a high thermal conductivity is a good material for the heat sink but it is extremely lossy for optics. Ideally, a thick Au layer should be placed close enough to the centre of the device while being sufficiently far away from the optical mode. Table 2.1 lists the core temperature of the device for different scenarios. As expected, the presence of the heat sink was definitely beneficial in bringing down the core temperature. In addition, the proximity of the thick Au sink improved greatly the heat extraction to achieve a lower core temperature. Having a thin-Au layer did not seem to have a significant effect, primarily due to the very small thickness of the layer. So, a thick layer of Au, placed close enough to the centre of the device, was considered the best choice.

**LASING MODE** The temperature profile obtained in above simulations was then used to define the change in refractive index of InP layer. The refractive index profile was, in turn, used to find the optical lasing mode.

Based on the thermal simulations, temperature profile along the radial direction was extracted for the model discussed above with  $1\ \mu\text{m}$  Au sink placed  $10\ \mu\text{m}$  from the centre. The overall shape

Temperature at the center of MEMS VCSEL	
$t_{Au-sink} = 1 \mu m, r_{DBR} = 7 \mu m$	
No heat sink	350 K
Au-sink placed with $D_{Au-sink} = 10 \mu m$	333 K
Au-sink placed with $D_{Au-sink} = 10 \mu m + \text{thin-Au}$	331 K
Au-sink placed with $D_{Au-sink} = 7 \mu m$	325 K
Au-sink placed with $D_{Au-sink} = 7 \mu m + \text{thin-Au}$	323 K

Table 2.1: Temperature at the center of the device for different heat sink configurations obtained on COMSOL.

of the temperature profile was similar to that of the pump beam profile (Gaussian in our case). The refractive index corresponding to the temperature profile was computed using the thermo-optic coefficient  $\partial n / \partial T$  of InP at 1550 nm. [26]

$$\partial n / \partial T = -2.17 \times 10^{-10} T^2 + 3.5 \times 10^{-7} T + 1.15 \times 10^{-4} (K^{-1}) \quad (2.14)$$

A simple 2D model based on graded index fibre was used for looking at the possible optical modes. Figure 2.20 shows the defined model. It consisted of two concentric circles with a core and cladding refractive index. The core corresponded to the computed refractive index (using Equation 2.14). The cladding had the same refractive index as the core refractive index at the boundary of the two regions. Mode analysis study using frequency domain electromagnetic waves physics was used for the simulation. The electric field outside the cladding layer was set to zero.

Figure 2.21 shows the fundamental mode for the defined model with an effective mode index of 3.166. The optical mode can be seen to be confined to the core. This, in a way, confirmed the working principle for thermal lensing. So, provided we have a well-defined pump beam, we can expect single mode lasing from the device. The second order modes were also obtained with effective mode index of 3.167.

The major assumptions in the thermal simulation were the input power to the laser and absorption in the active layer, which are dependent on the choice of material systems for the QW structure and optical setup (beam shape). The results obtained in this



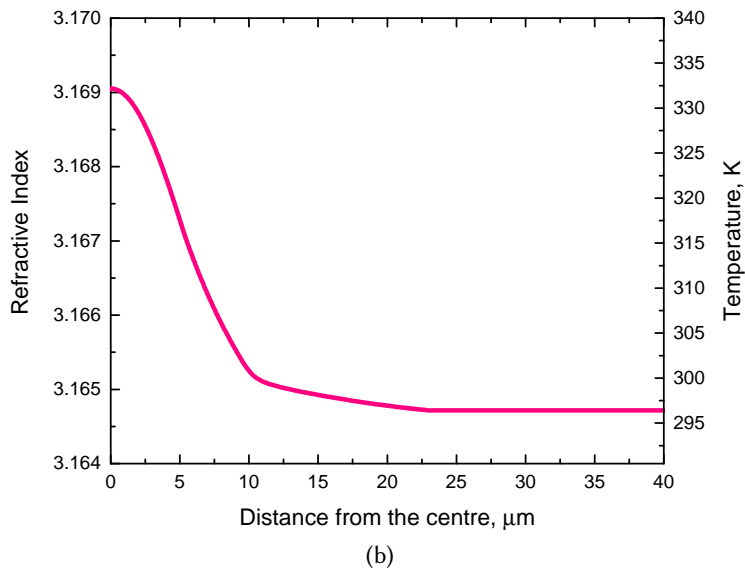
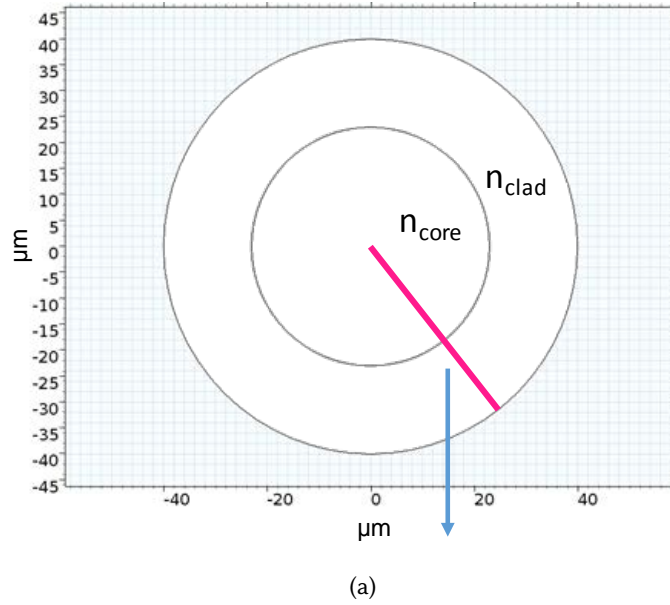


Figure 2.20: (a) 2D COMSOL model used for finding lasing modes corresponding to (b) the refractive index profile obtained from the temperature profile in the device.

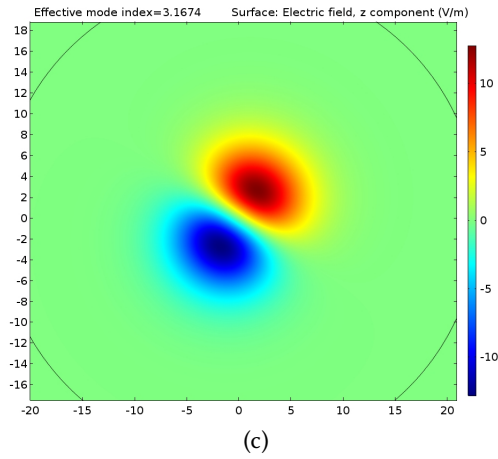
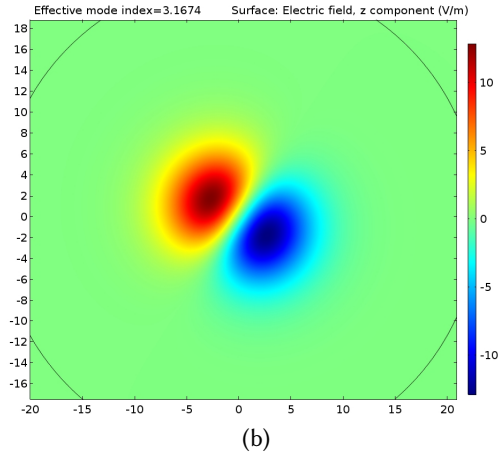
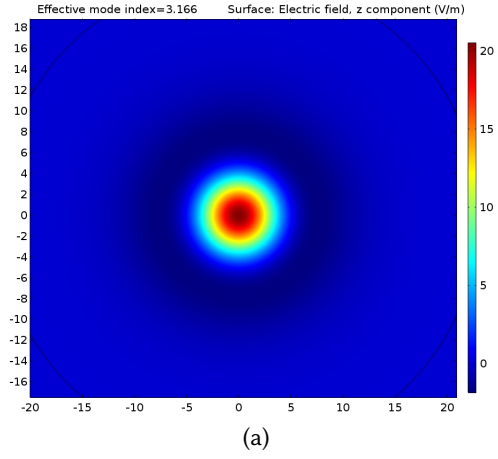


Figure 2.21: Fundamental (a) and second order (b and c) electric field modes shown corresponding to the model defined in Figure 2.20. The length scales are in  $\mu m$ .

section along with the assumptions will help in achieving a better understanding of the device.

## 2.4 ACTUATION

Electrostatic actuation was used for achieving tunability in the proposed device. Application of a voltage across two electrodes separated by an air gap creates opposite charges on the electrodes, which then creates a field directed from the positive electrode to the negative. The electrodes experience a force towards other. As the electrodes are connected to opposite polarities of the same voltage source, the force is always attractive in nature. For a voltage,  $V$ , applied across two electrodes (with an area of  $A$ ) separated by a gap  $d$ , the force,  $F_{el}$ , experienced by the electrodes is

$$F_{el} = \frac{\epsilon AV^2}{2d^2}, \quad (2.15)$$

where  $\epsilon$  is the permittivity of the medium. When one of the electrodes is fixed and the other is connected to a spring, there is an opposing spring force,  $F_{mech}$ , experienced by the latter electrode.

$$F_{mech} = k(d_o - d), \quad (2.16)$$

where  $k$  is the effective spring constant and  $d_o$  is the gap when no voltage is applied. The system reaches a stable state when the net force is zero, i.e.,  $F_{el} = F_{mech}$ . The effective gap in this state is

$$d = d_o - \frac{\epsilon AV^2}{2kd^2}. \quad (2.17)$$

The two forces ( $F_{el}$  and  $F_{mech}$ ) in the discussion do not depend on  $d$  in a similar fashion.  $F_{el}$  grows in a non-linear fashion and has a quadratic dependence on voltage unlike  $F_{mech}$ , which has a linear dependence on  $(d_o - d)$ . So, after a certain distance  $F_{mech}$  cannot match  $F_{el}$ . At gap smaller than  $\frac{2}{3}d_o$ ,  $F_{el}$  becomes stronger than  $F_{mech}$  and the movable electrode collapses on the fixed electrode [24, 87]. The corresponding voltage is termed as pull-in voltage,  $V_{pull-in}$

$$V_{pull-in} = \sqrt{\frac{8kd_o^3}{27\epsilon A}}. \quad (2.18)$$

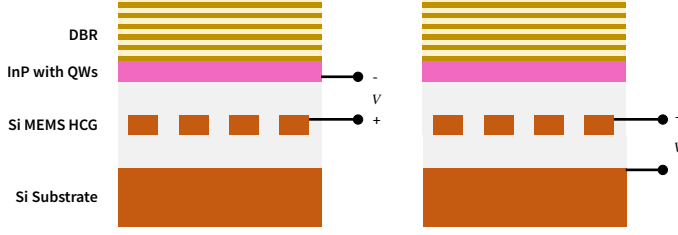


Figure 2.22: Electrostatic actuation scheme for tuning wavelength. The MEMS HCG can either be moved up (Left) or down (Right) based on the electrodes being used.

Thus, any voltage below  $V_{Pull-in}$  (i.e.  $d < \frac{2}{3}d_0$ ) is safe to operate. This limits the actuation distance (as mentioned earlier in section 2.2.3) and thus the maximum achievable tuning range is a third of initial gap. So, the cavity length, which is defined by the distance between the mirrors, is coupled closely with the desired tunability in the existing MEMS VCSEL designs. However, in the proposed design, the tuning range and cavity length can be de-coupled by pull away design (discussed in next section).

The mechanical design also plays an important role in actuation as evident from the equations 2.17 and 2.18. Figure 2.23 shows the mechanical element design of the device. It is a standard stage design to achieve conformal z-axis actuation. The centre of the stage contains HCG mirror. The stage is connected by four arms to fixed supports. The four arms define the spring constant for the system. In other words, the stage is connected by four fixed-guided beams, in parallel. The effective spring constant,  $k$ , for the system is

$$k = 4 \frac{Ewt^3}{L^3}, \quad (2.19)$$

where  $w$  is the width and  $L$  is the length of each beam,  $E$  is the Youngs modulus of Si, and  $t$  is the thickness of the Silicon layer.

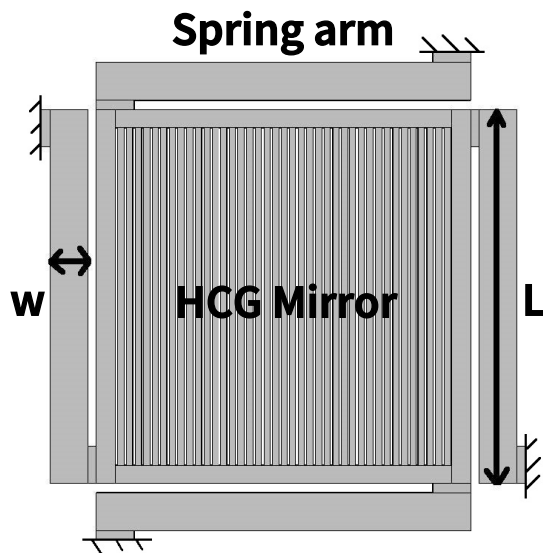


Figure 2.23: Illustration of the MEMS stage with HCG mirror.

#### 2.4.1 DC Tuning

Figure 2.22 shows the actuation schemes for the proposed device. There are three electrodes in the design: doped InP layer, Si MEMS layer and Si substrate. Application of a voltage between the top layers should move the MEMS close to the InP and we should see a blue shift in wavelength. This is similar to the actuation schemes on existing MEMS designs. When a voltage is applied between the bottom two layers, the cavity length is decoupled from tuning. In this case, MEMS can be placed as close as desired to the QWs in InP and tuning is achieved by pulling the MEMS HCG away from the device. The wavelength will red shift. In the fabricated device, the aim is to demonstrate two-way tuning. So, top airgap was kept big-enough to achieve tuning in both directions.

#### 2.4.2 AC Tuning

Speed and tuning range are important for OCT systems. For an oscillating mechanical system, the maximum displacement is achieved at the mechanical resonance frequency of the system. AC actua-

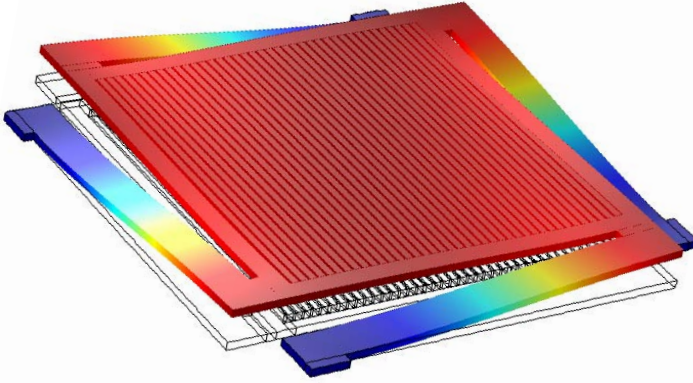


Figure 2.24: Fundamental mode shape of the model at eigenfrequency of 886 kHz.

tion will thus be aimed at finding the resonance frequency of the system and the tuning range. This will provide an indication of the maximum speed of operation without compromising on the tuning range.

It was also important to ensure that the MEMS element stayed conformal, i.e., parallel to the substrate in order to maintain the desired reflectivity. So, the mechanical element illustrated in Figure 2.23 was modelled on COMSOL to find its fundamental mechanical frequency and mode shape. Figure 2.24 shows that for 410 nm thick MEMS stage with beam dimensions of  $L = 20 \mu\text{m}$  and  $w = 2 \mu\text{m}$ , the fundamental eigenfrequency is 886 kHz. It has a good conformal shape which is as desired. The mechanical resonance of MEMS stage was determined under the assumption that the element is in free space. However, for the proposed device, the element is in a cavity with a certain pressure and volume. This may influence the measured resonance frequency.

## 2.5 CHALLENGES

The simulations verified working of the device and provide the essential parameters for fabricating the device. However, one of the

crucial steps to realizing the device is the integration of SOI wafer with InP (III-V).

There are many options to bond - metal-based bonding, adhesive/polymer based bonding or direct bonding. Using metals to bond require adding metal onto the chip half way through the fabrication process and it is not desirable. Most fabrication tools (etch/deposition) like to avoid metals citing contamination. So, as a good practice, metal deposition is generally pushed to the end of the process flow. In addition, there is also need for good alignment. Next, polymer-based bonding will require spinning a polymer like Benzocyclobutene (BCB) on the entire wafer, which is not good as it will fill the MEMS cavity. Also, having polymer everywhere will mean undesired material along the optical path. Further, the thickness and quality of the polymer will be greatly dependent on the processing parameters like temperature, pressure etc. and e.g. prohibit epitaxial regrowth after bonding. This narrows down the search to direct-bonding, which promises a clean integration process free of any metal or adhesives. However, it is very heavy on its requirements of a clean, ultra-smooth surface with the need for high-temperature annealing.

Nevertheless, direct-bonding is a clean integration process and is a great match for the proposed device. However, there has been a limited study on the method. Most of the work has been focused on Si bonding to realize SOI wafers. So, the next chapter will revisit the working principle and optimize the process flow for bonding InP with SOI wafer.

## Part II

### THE CRAFT





## BONDING

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Bonding of active material to an silicon on insulator (SOI) wafer (with microelectromechanical systems (MEMS) high contrast grating (HCG)) was an important step for realizing the proposed tunable MEMS vertical-cavity surface-emitting laser (VCSEL) . This chapter discusses the use of a very thin layer of  $\text{Al}_2\text{O}_3$  as an intermediate layer for low temperature direct wafer bonding. It presents a systematic study on optimizing the interface energy for  $\text{Al}_2\text{O}_3$  based wafer bonding. Lastly, the chapter outlines an optimized bonding process flow.

### 3.1 IMPROVING DIRECT BONDING

Direct bonding is a better and cleaner choice against polymer adhesive bonding or eutectic bonding or anodic bonding etc. The requirement for a good direct bonding is to have an ultra-clean, smooth hydrophilic surface. When bondable wafer surfaces are brought in contact with each other at room temperature, the two surfaces are held together using hydrogen bonds. An annealing step usually follows to form covalent links between the two wafer surfaces.

#### 3.1.1 *Direct Bonding*

Direct wafer bonding is a key enabling technology for many current and emerging nanophotonic devices. Most of the work on direct wafer bonding has however been focused on the Si platform for fabrication of SOI and MEMS. The work on direct wafer bonding of Si to Si/SiO<sub>2</sub> using high temperature annealing from Maszara et al. [60] is one of the earliest efforts on understanding bonding. Tong and Gösele [100] furthered the understanding by investigat-

ing the contribution of hydroxyl groups and achieved a high interface energy by increasing annealing time. These works remain the gold standards for direct bonding. Adapting the bonding process to heterogeneous materials is, however, a challenge. First, high temperature annealing of hetero bonded samples gives rise to thermal stress in the film or even defects due to mismatched coefficients of thermal expansion. For example, annealing of InP bonded to Si at a temperature above 300 °C leads to a build-up of internal stresses in the bonded wafers which creates defects in the InP wafer. [75] Integration of heterogeneous materials thus remains one of the roadblocks for semiconductor devices on new platforms such as III-V on Si and Germanium (Ge) on Sapphire and LiNbO<sub>3</sub> on gallium arsenide (GaAs). Second, it is important to maximize the density of bond sites, i.e., the hydroxyl group density for a strong bond. A common way to achieve this is to break the surface bonds by O<sub>2</sub> plasma, Ar sputtering, etc. on a wafer followed by a dip in deionized water (DIW) to re-hydrolyze the surface. This method has a few drawbacks and cannot be adapted to all systems. The process of breaking surface bonds increases surface roughness. [4, 74] Also, dipping in water is not desired, especially when you have MEMS and there is a risk of damaging them. In addition, the maximum hydroxyl group density on a wafer surface is an intrinsic property of the material and thus cannot be increased beyond a certain limit for the desired material. Thus, adapting the Si-Si bonding process to a new material platform does not necessarily guarantee an acceptable bond quality. These concerns have generated a strong interest in finding an alternative solution for bonding of heterogeneous materials at low temperature.

### 3.1.2 *Al<sub>2</sub>O<sub>3</sub> based direct bonding*

The key to achieving a high interface energy at low temperature lies in the choice of a material with high hydroxyl group density and use that material as an intermediate layer for direct bonding. This would increase reliability and reduce the dependence on the substrate material for achieving a high interface energy. Al<sub>2</sub>O<sub>3</sub> is an excellent choice for an intermediate layer for direct bonding. It has a high hydroxyl group density of around 18 OH/nm<sup>2</sup>, [27, 101] more than four times higher than that of Si. [8, 113] Al<sub>2</sub>O<sub>3</sub> can

also be deposited with high accuracy using atomic layer deposition (ALD). The ALD process helps in achieving thickness control at the sub-nm scale and does not add any surface roughness. There have been some reports on  $\text{Al}_2\text{O}_3$  [31, 32, 45, 54] based bonding being stronger than Si/SiO<sub>2</sub> direct bonding. However, there is a lack of systematic studies to understand the bonding mechanism using  $\text{Al}_2\text{O}_3$  as the intermediate layer. In this work, we have investigated the contribution of deposition parameters for  $\text{Al}_2\text{O}_3$ , the thickness of  $\text{Al}_2\text{O}_3$ , and annealing conditions to the bond strength. Finally, an optimized process flow for bonding heterogeneous materials is presented; the process can be applied to most material systems.

### 3.2 METHODOLOGY

Characterization is important for the ability to quantify a good bond. It can be either a quantitative or qualitative measurement. Common quantitative wafer bond characterization methods include Maszara's blade test, [60] and micro-chevron test. [76] Despite high reliability of the latter, the Maszara test is the most used method, [23, 55, 81, 86] because of its simplicity and ease of use. Masteika et al. [59] have identified some of the common mistakes and articulated the correct methodology for an accurate Maszara test. Even so, brittleness of some of the wafers (InP, GaAs, etc.) makes it a challenge to do any of the above-mentioned tests. On the other hand, qualitative measurement refers to the ability of the bonded sample to survive polishing or substrate removal etch. It does not sacrifice the sample, unlike the quantitative methods. So, for expensive wafers such as InP, GaAs, sapphire and LiNbO<sub>3</sub>, the most common characterization method has been qualitative. This has resulted in an incomplete knowledge of the bond quality and the mechanism behind a successful bonding. Thus, to be able to characterize and understand  $\text{Al}_2\text{O}_3$  based direct bonding, Si wafers were chosen for the experiment. This helped us benchmarking our approach against the standard Si direct bonding with high annealing temperatures. Bonding is primarily a surface phenomenon and depends entirely on the forces between the bonding surfaces. Apart from stress from the wafer, there is almost no contribution from the underlying material. Thus, any result obtained

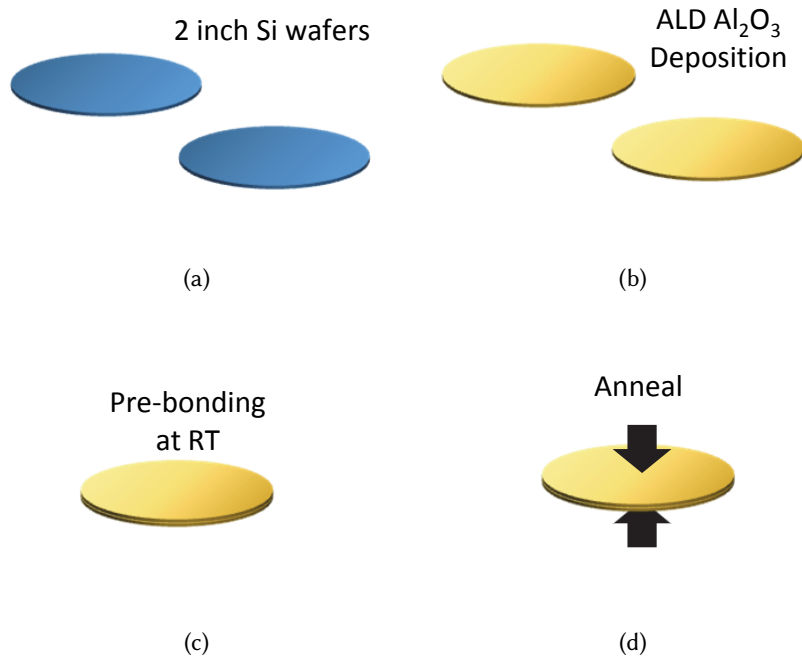


Figure 3.1: Basic steps followed for bonding wafers using  $\text{Al}_2\text{O}_3$  as an intermediate layer are illustrated above. (a) Two prime grade 2 inch clean Si wafers with surface roughness around 0.2 nm were chosen in this experiment. (b) A thin layer of ALD  $\text{Al}_2\text{O}_3$  was deposited on both wafers. (c) The wafers were then placed on top of each other for the pre-bonding. An additional exposure to water vapor, before the pre-bonding was done for one experiment run to understand the effect of hydroxyl density and temperature. (d) The wafers were finally annealed at a low temperature ( $\leq 300^\circ\text{C}$ ) and a controlled applied pressure.

from bonding of Si wafers using  $\text{Al}_2\text{O}_3$  as the intermediate layer can be adapted to most material systems.

The basic bonding steps are illustrated in the Figure 3.1. Two prime grade single crystal (100) 2-inch clean Si wafers with a surface roughness of around 0.2 nm were used for each run. The wafers were taken out of a new sealed wafer box and ALD  $\text{Al}_2\text{O}_3$  was deposited on both wafers. The deposition process was done in a commercial thermal ALD system using liquid precursors trimethylaluminum (TMA) and DIW. A pulse time of 0.1 s was used for both TMA and  $\text{H}_2\text{O}$  with a nitrogen flow of 150 and 200 sccm respectively. The thickness of the deposited film was controlled by the number of cycles of ALD. The temperature for deposition was kept between 200 and 300 °C in-order to achieve a uniform and high quality deposition of  $\text{Al}_2\text{O}_3$ . [49, 61, 72] The deposition rate of  $\sim 1\text{\AA}/\text{cycle}$  was obtained in the operating temperature regime. The wafers were pre-bonded right out of the chamber. The wafers were placed on top of each other with the bondable surface facing each other and a small force was applied in the center of the wafers for initiating the bond wave. In some runs, the wafers were exposed to water vapor for 30 sec before pre-bonding, to study the effect of hydroxylation. The pre-bonded wafers were then annealed. The annealing step was done in a commercial wafer bonder. The annealing temperature was varied between 200 and 300 °C. The annealing temperature is specific to the materials being bonded. For example, the maximum allowed temperature for annealing an InP wafer bonded to Si would be 300 °C. An annealing time of 60 min was used for all runs except when the effect of annealing time was studied. A force of 2 kN was applied on the 2 inch bonded wafers during the annealing process. To investigate the contribution from applied pressure during annealing, some samples were also annealed in a furnace without any applied force. The bonded wafers were characterized using the Maszara blade test in a cleanroom atmosphere by measuring the de-lamination from the insertion of a 50  $\mu\text{m}$  thick steel strip between the wafers. Figure 3.2 shows an infrared image of the Maszara blade test on a bonded Si-Si wafers. The interface energy,  $\gamma$  was then calculated using [60]

$$\gamma = \frac{3}{32} \frac{Et^3y^2}{L^4}, \quad (3.1)$$

where  $E$  is Young's modulus of the material,  $t$  is the thickness of the wafers,  $y$  is the thickness of the blade and  $L$  is the crack length.

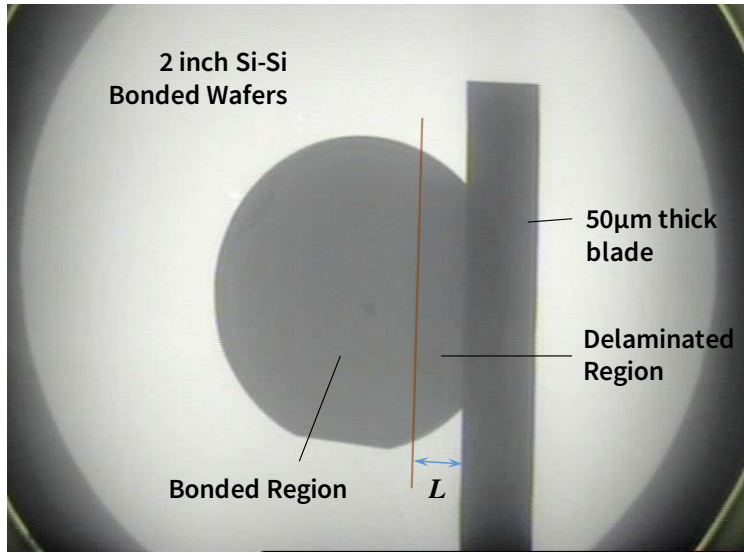


Figure 3.2: Infrared camera image with overlaid information obtained from the Maszara blade test.

Care was taken to use the correct value of  $E$  for Si [40] based on the direction of insertion of the blade relative to the wafer flat. The experimental error for the measurement method is typically  $\pm 15\%$  due to variations on the wafer surfaces and crack length measurement procedure. In the results shown below, the error bars represent the standard deviation of the measurements.

### 3.3 INSIGHTS

#### 3.3.1 Thickness of ALD $\text{Al}_2\text{O}_3$

The amount of  $\text{Al}_2\text{O}_3$  required for use as an intermediate layer for direct bonding is very important. It would be desirable to have as little as possible and at the same time not to compromise on the bond quality. In our case [84] where ALD  $\text{Al}_2\text{O}_3$  would be deposited even on the mechanical structure, it is critical to have as thin a layer as possible in order not to alter the mechanical properties of the structure. On the other hand, the amount of material should not be too small for an effective bond.

To study the amount of  $\text{Al}_2\text{O}_3$  required for a good bond, the number of ALD cycles was varied from 25 to 500 cycles ( $\sim 2\text{-}50\text{ nm}$ ). The minimum number of cycles was chosen as 25 cycles to ensure a uniform deposition [66, 91] on the whole wafer. The upper limit was chosen to be 500 cycles to test bond-ability with a thick layer of  $\text{Al}_2\text{O}_3$ . Figure 3.3 shows the interface energy measured for wafers bonded with different thicknesses of the intermediate material. For all thicknesses below 300 cycles, almost no appreciable change in interface energy was observed. This agrees with our earlier discussion on bonding as a surface phenomenon. So, an intermediate layer as thin as 2 nm  $\text{Al}_2\text{O}_3$  should be enough for a successful bond. The samples with 50 nm of ALD  $\text{Al}_2\text{O}_3$ , however, showed slightly lower interface energy. It is remarkable that very good bonding strength is obtained in all cases, since the native oxide is known to be too thin [78, 102, 104] to accommodate the hydrogen molecules that are usually evolved during annealing. Hydrogen is evolved due to oxidation of silicon by water arising from the reaction of the surface hydroxyl groups. Hydrogen is expected to form bonding defects in the form of interface bubbles,[104] which reduce the bonding strength. We suggest that the native oxide (annealed in the ALD process) and the much denser  $\text{Al}_2\text{O}_3$  film [52] in combination prevents diffusion of water to the silicon interface and thus hydrogen evolution is avoided. Ventosa et al.[103] showed that annealing of the native oxide could prevent hydrogen evolution and lead to void-free bonding.

Thus, a few nm of ALD  $\text{Al}_2\text{O}_3$  (2 nm, to ensure uniform coverage) can be used as an intermediate layer to achieve a good bond. So, an optimized 25 cycles of ALD  $\text{Al}_2\text{O}_3$  were used for the next experimental runs.

### 3.3.2 Density of (-OH) groups

As mentioned earlier, high hydroxyl group density is responsible for robust bond formation as also highlighted in the literature [59, 100] on low temperature bonding mechanisms. The pre-bond step brings bondable surfaces in close proximity and a weak hydrogen bond is formed between the two surfaces. With annealing, these sites would give way to the formation of Al-O-Al thereby chemically binding the two surfaces. So, the process flow should be op-



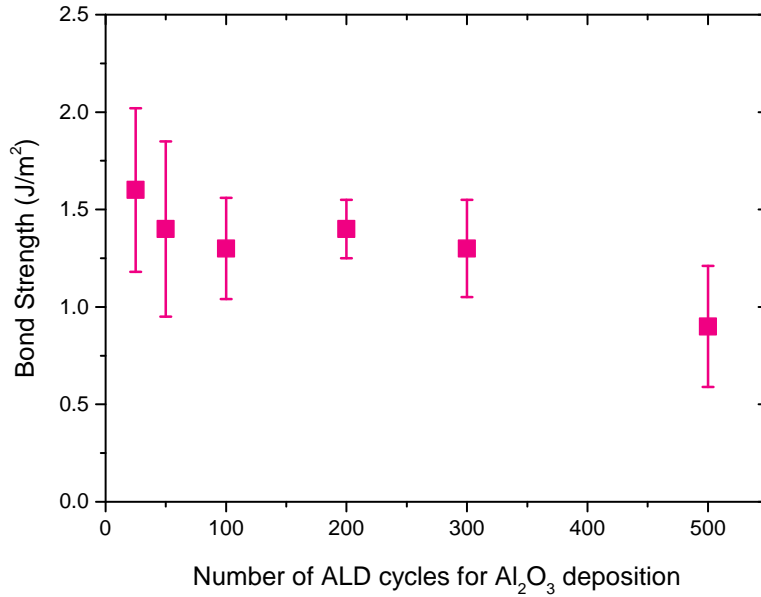
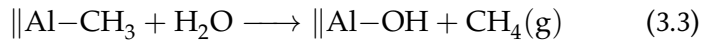
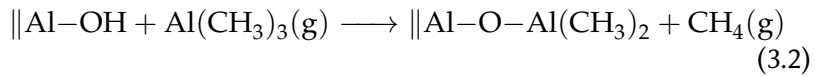


Figure 3.3: Interface energy of Si wafers bonded using different thickness of Al<sub>2</sub>O<sub>3</sub> as intermediate layer. Al<sub>2</sub>O<sub>3</sub> was deposited using ALD at 200 °C. The deposition rate is  $\sim 1$  Å/cycle. The samples were annealed at 300 °C for 60 min. The symbols represent the average interface energy and bars represent the standard deviation in the measurements.

timized for maximizing the hydroxyl group density on the wafer surface. In this case, the ALD deposition process for Al<sub>2</sub>O<sub>3</sub> decides the surface chemistry. The process of ALD deposition can be described by the following equations [28, 79, 89]



where  $\parallel$  implies the top surface of the wafer.

The first reaction with TMA is irreversible and is not affected by the temperature within the reaction temperature regime. [79] The second step, hydroxylation of the surface is often mentioned without a competing reaction, which is a temperature dependent step and is a reversible reaction (Equation 3.4). [49, 80] At high temper-

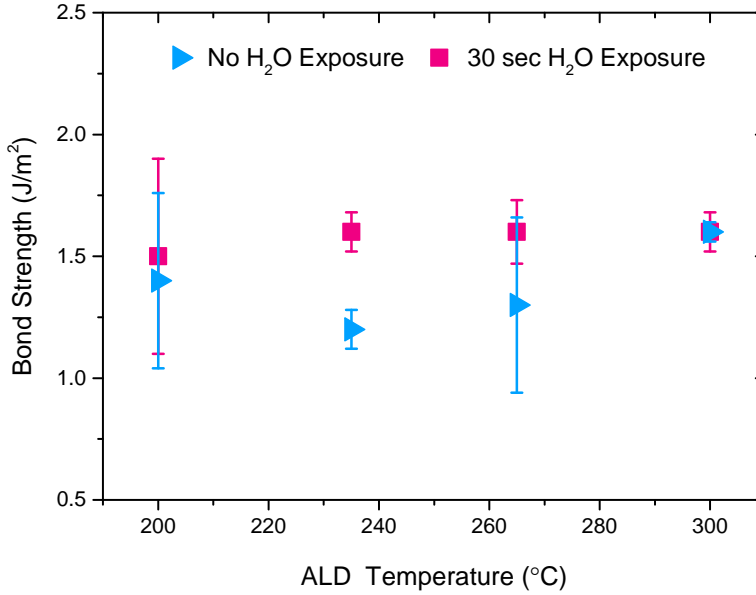
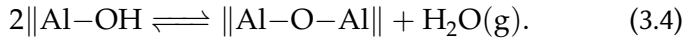


Figure 3.4: Interface energy of Si wafers bonded using  $\text{Al}_2\text{O}_3$ , deposited at different temperature, with (squares) or without (triangles) a 30 sec  $\text{H}_2\text{O}$  exposure between unloading of wafers from the chamber and pre-bonding. All the samples were annealed at 300 °C with a force of 2 kN on 2 inch full wafers. The symbols represent the average interface energy and bars represent the standard deviation in the measurements.

atures, the hydroxy groups from the surface ( $\text{Al}-\text{OH}$ ) may react with each other (Equation 3.4) and thus reduce the number of hydroxy groups on the surface



So, to test the effect of the dehydroxylation temperature dependent step, 25 cycles of ALD  $\text{Al}_2\text{O}_3$  were performed at different temperatures between 200 and 300 °C. In another set of parallel runs, the wafers were unloaded from the ALD chamber and were exposed to water vapor for 30 sec before being brought in contact with each other. This process step was included in an effort to re-hydrolyze the surface. In all the above runs, the wafers were not settled on any heat sink.

Figure 3.4 shows the interface energy measured for wafers bonded with 2 nm of  $\text{Al}_2\text{O}_3$  intermediate layer deposited at different ALD

temperatures. The first set of runs where the temperature of deposition was the only variable, there is no appreciable difference in the interface energy. Even though a decrease in the interface energy with ALD deposition temperature is expected due to decreased hydroxyl density, the temperature regime for the experiments is most likely too narrow to show any profound effect. The second set of runs which included an added 30 sec exposure to water vapor definitely shows a small increase in interface energy relative to the first set of runs. Furthermore, the interface energy for these runs is independent of the ALD deposition temperature. Thus it can be concluded that while ALD deposition temperature has a direct influence on the hydroxyl group density on the wafers, a short exposure to an atmosphere with high relative humidity will help restore some of the hydroxyl groups. To further improve the process, ALD  $\text{Al}_2\text{O}_3$  deposited wafers should be put on a metal plate (heat sink) to bring the wafer temperature to room temperature in an atmosphere with a relative humidity of 50 % (standard clean-room). This should help increase the hydroxyl group density.

### 3.3.3 *Annealing Parameters*

Annealing of bonded samples helps increase the interface energy. There are three important parameters - annealing temperature, applied pressure and annealing duration. With higher annealing temperatures, the interface water molecules become more mobile and lead to a change from hydrogen bonding towards covalent bonds. Applied pressure helps bring the wafer surfaces closer and might contribute to increasing the bond quality. Equally important is the duration of annealing, which roughly translates to the time assigned for the above-mentioned mechanism to occur.

In order to optimize the annealing parameters, the pre-bonded wafers were annealed at 200 and 300 °C, with/ without applied pressure and the annealing duration was varied from 1 hr to 20 hr. The annealing temperature was limited to 300 °C to be compatible with heterogeneous bonding. The applied pressure was limited by the maximum allowed force on the commercial wafer bonder. The annealing time was restricted to 20 hr due to the limited availability of the wafer bonder. Figure 3.5 confirms that with an increase in annealing temperature, there is an observed increase in the interface

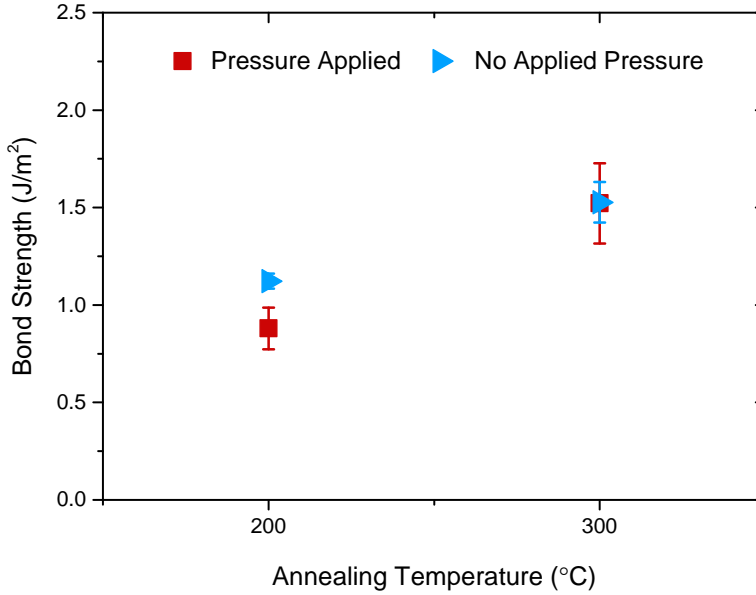


Figure 3.5: Interface energy of Si wafers bonded using  $\text{Al}_2\text{O}_3$  as the intermediate layer and annealed at different temperatures with/without the application of pressure (15 kN on 2 inch wafer) for 60 min. The increase in temperature increases the interface energy but there is no observed effect of applied pressure during annealing.

energy. Applied pressure does not have any appreciable effect on the interface energy. However, in spite of this experimental result, small particles might get trapped due to wafer handling and an applied pressure would help to reduce the size of voids formed due to them. Finally, Figure 3.6 shows that the interface energy does not change with annealing time, at least for 20 hours duration used in this experiment.

#### 3.3.4 Optimized process flow

The above-discussed results help in proposing an optimized bonding process using  $\text{Al}_2\text{O}_3$  as the intermediate layer. Initially, the requirement on cleanliness and surface roughness remain almost the same as that of direct bonding, except there is no need for standard wet cleaning steps (RCA, Piranha, etc). Proper handling

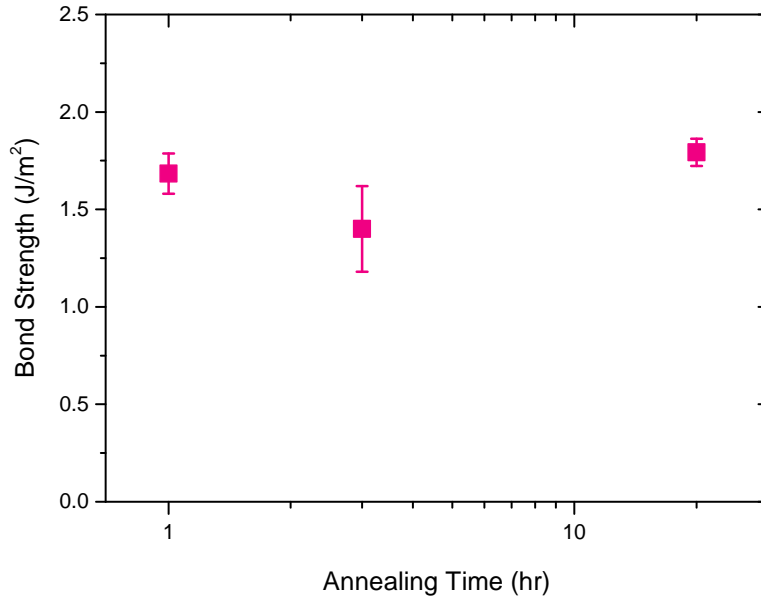


Figure 3.6: Interface energy of Si wafers bonded using  $\text{Al}_2\text{O}_3$  deposited at 200 °C as the intermediate layer and annealed at 300 °C for different durations. There was no significant change in the interface energy when the annealing time was increased from 1 hr to 20 hr.

should be ensured to minimize contamination. Next, as deduced from Figure 3.3, the wafers are coated with a thin layer ( $\sim 2$  nm) of ALD  $\text{Al}_2\text{O}_3$ , deposited at 200 °C. The wafers are bonded right after unloading from the ALD chamber with no additional activation step. The wafers may, however, be placed on a heat sink for some time to maximize the hydroxyl coverage. Finally, the wafers are to be annealed at highest permissible temperature with an application of small force for 60 min. The bonded wafers are expected to have a high interface energy of around 1.7 J/m<sup>2</sup>. The annealing time, in particular, can be further optimized to achieve a saturated interface energy as reported in Tong and Gösele [100]. An extended anneal can be used after an initial anneal under pressure. Figure 3.7 shows the interface energy obtained in this work benchmarked against Si-Si direct bonding with annealing time of 1 hr [60] and 100 hr, [100] respectively. The achieved interface energy was high enough for our requirements (surviving substrate removal and post-processing).

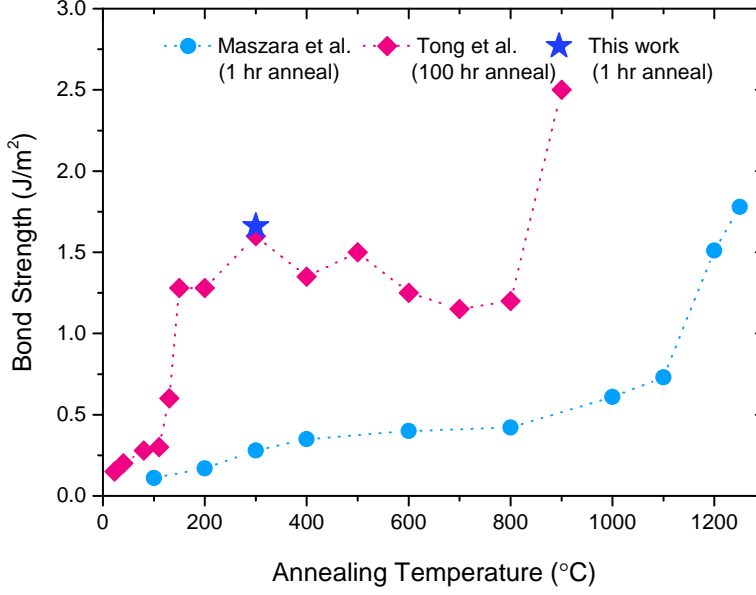


Figure 3.7: Interface energy of Si-Si wafers bonded using  $\text{Al}_2\text{O}_3$  as the intermediate layer annealed at 300 °C for 1 hr, bench-marked against direct Si-Si bonding annealed for 1 hr (Maszara et al.[60]) and 100 hr (Tong and Gösele [100]).

### 3.4 BONDING HETEROGENEOUS MATERIALS

The optimized process flow, mentioned above, was successfully applied to two different hetero wafer systems. A 2 inch InP wafer was bonded to thermal oxide grown on a Si wafer and a 2 inch GaAs wafer was bonded to a sapphire wafer. After the bonding, the III-V substrates were etched away until a stop layer, thus leaving less than a micron of InP or GaAs behind (Figure 3.8). The ability to survive the etch is used by many experimentalists as a qualitative test for the bonding. The voids visible on the wafers are from particles on the wafers before bonding. In another run, a patterned wafer ( $\sim 1 \mu\text{m}$  steps of  $\text{SiO}_2$  on a Si wafer) was bonded to InP. A cross-sectional image of the cleaved wafer is shown in Figure 3.9. The wafers have been processed further towards interesting nanophotonic devices. For these wafers, the Maszara test could not be performed since the high interface energy made III-V wafers break instead of delamination.

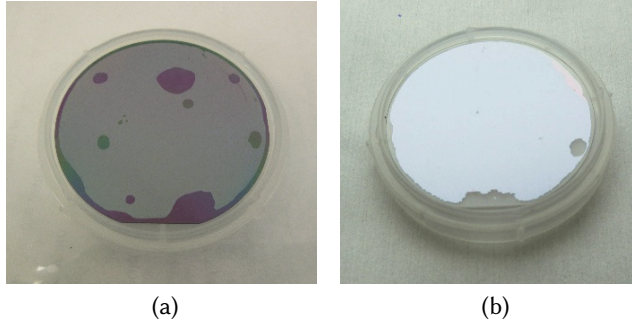


Figure 3.8: Images of 2-inch bonded wafers. (a) InP bonded to  $\text{SiO}_2$  on Si and (b) GaAs bonded to sapphire after a III-V substrate etch process.

### 3.5 SUMMARY

We have investigated and optimized a low temperature bonding process using  $\text{Al}_2\text{O}_3$  as an intermediate layer to bond InP (active material) with SOI wafer.  $\text{Al}_2\text{O}_3$  is an excellent choice for the intermediate layer since it has a high hydroxyl group density. We investigated the contribution of the ALD  $\text{Al}_2\text{O}_3$  thickness, deposition temperature and annealing parameters in order to achieve a high interface energy. We also avoided wet processing or any separate activation steps before bonding which was essential for the proposed device. An interface energy of  $1.7 \text{ J/m}^2$  was achieved for Si-Si bonding using  $\text{Al}_2\text{O}_3$  as the intermediate layer after annealing for 1 hr at  $300^\circ\text{C}$ . The value is higher than the saturated interface energy for Si-Si direct bonding after annealing at  $300^\circ\text{C}$ . Finally, we also demonstrated adaptation of the bonding process to two hetero-material platforms.

The presented bonding process technology is also expected to find application in the integration of III-V on Si, Ge on sapphire,  $\text{LiNbO}_3$  on GaAs, etc. and thus paving the way for a new family of devices.

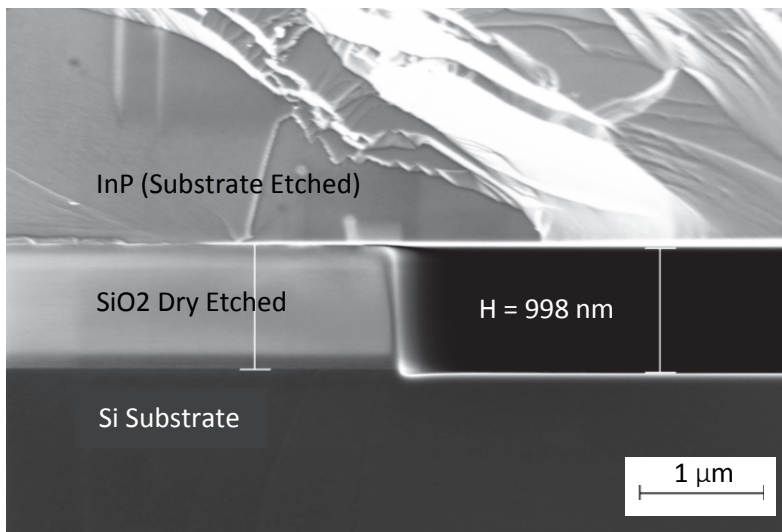


Figure 3.9: Cross-sectional SEM image of a bonded interface. Patterned SiO<sub>2</sub> on Si using dry etch was bonded to InP wafer with Al<sub>2</sub>O<sub>3</sub> as an intermediate layer.





## FABRICATION

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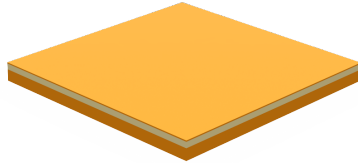
Fabrication of the proposed microelectromechanical systems (MEMS) vertical-cavity surface-emitting laser (VCSEL) was another big milestone for realizing the device. Since the design was different from earlier MEMS VCSEL [6] from the Nanophotonics group at DTU, many new process flows had to be established, bonding of III-V to Si being one of them. The complete process flow involved many Si and InP processing steps which meant the complete process flow was long. The processing steps were also dependent on each other, because of which, many long iterations were required to optimize processing for the device. This chapter aims to describe the optimized process flow and discuss some of the experiments used for optimization. To simplify the description, the process flow is divided into 3 different phases. Phase I discusses the Si-based processing on an SOI wafer for the definition of MEMS HCG structure. Phase II covers bonding of structured SOI wafer to an InP wafer and processing on the bonded wafer to define contacts for actuation (tuning). Lastly, Phase III discusses deposition of the top mirror (dielectric DBR).

Fabrication process flow of a tunable MEMS VCSEL for 1550 nm is discussed in this chapter. A more detailed fabrication is presented in Appendix A.

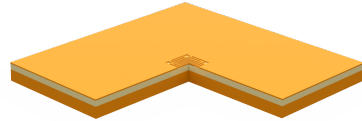
### 4.1 PHASE I: HCG AND SPACER DEFINITION

Two kinds of wafers were used for the fabrication process - a SOI wafer and an InP wafer with QW structures. Phase I (Figure 4.1) primarily constitutes the definition of the bottom mirror on a SOI wafer followed by definition of air-gap on top of the MEMS with the help of a spacer layer.

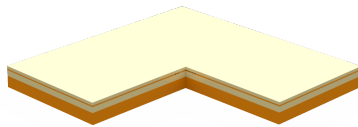
SOI wafers were ordered from IQE Silicon (Appendix A.1). The SOI wafers had 410 nm p-doped Si layer and 1  $\mu\text{m}$  buried oxide. The thickness of the Si layer was decided based on HCG simulations



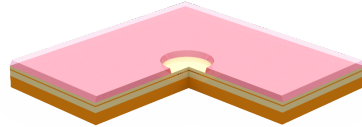
(a) RCA Cleaning on SOI wafer



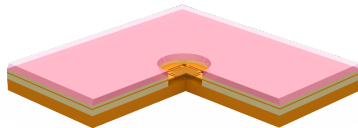
(b) MEMS HCG definition on Si layer



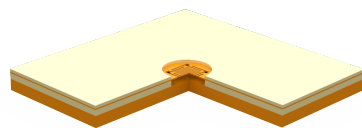
(c) Blanket deposition of  $\text{SiO}_2$  and PBSG



(d) Resist mask to open up area above HCG



(e)  $\text{SiO}_2$  (dry + wet) etch to define the air-gap and release MEMS



(f) Resist strip

Figure 4.1: Phase I fabrication steps

(Section 2.3.2) for high reflectivity around the lasing wavelength (1550 nm). The doping ensured a near-ohmic contact for MEMS actuation.

Ideally, 2-inch SOI wafers would have been the best choice which would have complemented the standard 2 inch InP wafers. Unfortunately, 2-inch SOI wafers with custom thickness and doping profile are difficult to find. An alternative option was to work with cleaved pieces but then there was the challenge of dealing with particles from cleaving (which was very crucial for good bonding). So, 6-inch SOI wafers were bought and at a certain point during the process, the 6-inch wafer was cleaved as per the requirement. The decision on when and how to cleave the wafer was dictated by the need to minimize particles and contamination.

#### 4.1.1 *Cleaning*

Wafer cleaning is an important component of cleanroom fabrication. So, it was done wherever possible and the first step for the process flow was RCA cleaning. One 6 inch SOI wafer was cleaned using standard RCA1 + RCA2 at 70°C. (Refer Appendix A.2) RCA1 removes the organics and RCA2 removes traces of metal. A brief 30 sec buffered hydrofluoric acid (bHF) dip was also done at the end to remove native oxide. The wafer was then moved to a clean box and prepared for the next step: HCG patterning.

#### 4.1.2 *HCG Patterning*

E-beam lithography was used for defining the HCG mirror along with the MEMS structure on the cleaned SOI wafer. E-beam patterning was chosen in order to achieve sub-micron structures with high precision. deep ultraviolet (DUV) lithography was an alternative but was not considered because of established process knowledge in the research group on e-beam exposure and relatively simpler processing.

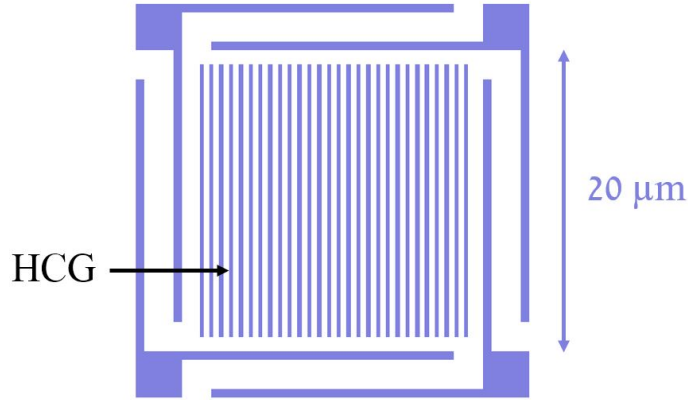


Figure 4.2: E-beam pattern of HCG on a MEMS frame of  $20\ \mu\text{m}$  side length. An array of this pattern with variations frame size and shape, and HCG duty cycle and period were exposed.

#### 4.1.2.1 *Ebeam Exposure*

The exposed pattern was an array of Figure 4.2. The centre of the pattern is a HCG mirror and it sits on a frame/stage which is connected by 4 arms to the Si layer. There were many variations included in the design, both related to MEMS stage and HCG. The size of the MEMS frame and width of its arms were varied to study the mechanical dynamics. The HCG duty cycle, on the other hand, was varied to address any fabrication imperfections during dry etch process (Section 2.3.2). Details on the process parameters for e-beam exposure can be found in the Appendix A.3.

Due to time constraints, only square frames with side length  $20\ \mu\text{m}$  were studied. So, the thesis will focus only on that.

#### 4.1.2.2 *Silicon RIE*

The exposed e-beam pattern was transferred to silicon MEMS layer using reactive-ion etching (RIE) process on SPTS Pegasus (Figure 4.3). (See A.4 for more details). The etch process was a continuous slow etch done at  $-20^\circ\text{C}$  in order to enhance the anisotropy and achieve the desired grating dimensions.

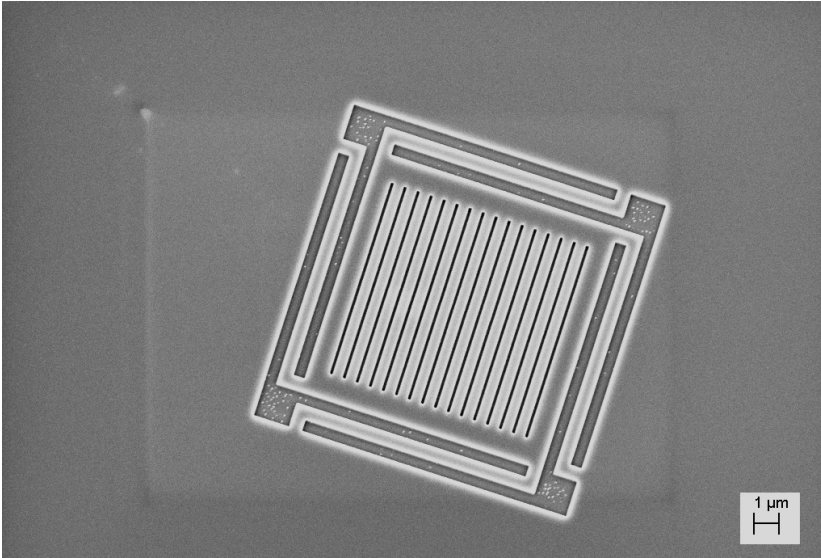


Figure 4.3: SEM Image the etched MEMS structure with HCG mirror on Si.

At this point, the wafer was cleaved into 4 pieces for further processing. Each piece was eventually bonded to a 2-inch InP wafer as shown in Figure 4.4.

The resist mask was cleaned away using oxygen plasma for 20 min. In some runs, 15 min of sonication cleaning was added in order to remove any silicon dust from the cleaving step. Then, it was RCA cleaned (Appendix A.2), which was also the last wet cleaning for the device before bonding. The next steps defined a spacer layer and released MEMS. Any wet processing after that would have damaged the MEMS.

#### 4.1.3 $\text{SiO}_2$ Spacer

After etching the MEMS frame with the HCG onto Si, a spacer layer with an air-gap opening on top of the MEMS was defined.  $\text{SiO}_2$  was chosen as the spacer layer as it is a relatively easy material to work with. It is good for electrical insulation between the Si MEMS layer and the InP layer. Further, it is a standard material for CMOS industry with a lot of established processing.

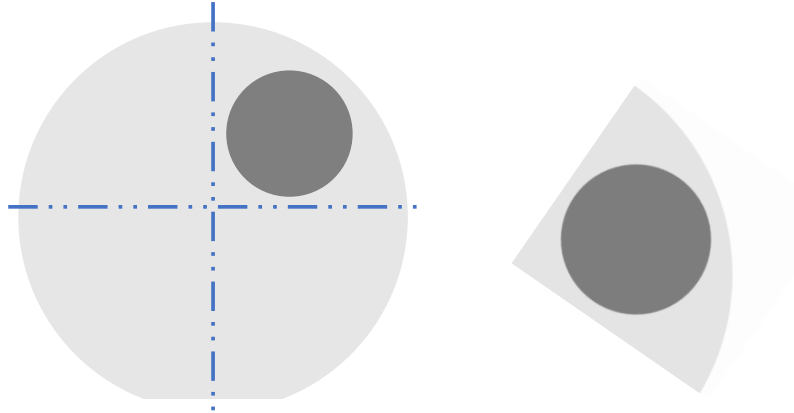


Figure 4.4: Illustration showing the cleaving lines for a 6 inch wafer and the relative size of each part with respect to a 2 inch wafer.

From a design perspective, the spacer layer brings in a great amount of flexibility in deciding the cavity length (air-gap). For our design, we could have chosen a thin spacer layer and just use pull away design. Thus, we would have a large FSR this way. We decided to have a thicker spacer layer and thus have the possibility to tune both ways. The correct spacer thickness was determined by device simulation as discussed in section 2.3.3.

#### 4.1.3.1 *SiO<sub>2</sub> Deposition*

The spacer layer was defined by deposition of SiO<sub>2</sub> and phosphorus boron silicate glass (PBSG) followed by annealing at 1000 °C. The choice to deposit two types of SiO<sub>2</sub> was done in order to achieve a required surface roughness (< 0.3 nm), which is essential for a good bond.

Two common ways to deposit thick SiO<sub>2</sub> at DTU Danchip are: plasma-enhanced chemical vapor deposition (PECVD) SiO<sub>2</sub> or low pressure chemical vapor deposition (LPCVD) tetraethyl orthosilicate (TEOS). The best surface roughness achieved in both depositions were not good for bonding (Figure 4.5). So, the search was extended to PBSG. PECVD deposited PBSG can be reflowed to achieve a very smooth surface (~0.2 nm).

While PBSG helped in achieving a smooth surface, it is a not an easy material to work with. It adsorbs water quite fast. So, it should be annealed right after deposition. In addition, it is a difficult material to etch using bHF, which was used later in the process flow. In order to work around the issues, the total spacer thickness (930 nm), thus, was divided between PECVD SiO<sub>2</sub> (300 nm) and PECVD PBSG (630 nm). PBSG deposited on the top helped achieve a very smooth bondable surface and PECVD SiO<sub>2</sub> underneath acted as a buffer layer for dry etching PBSG, which is discussed in the next section. (See Appendix A.5 for more details.)

#### 4.1.3.2 *SiO<sub>2</sub> Etch*

Next, in order to define air-gap on top of the MEMS and release the MEMS structure, there were three different types of SiO<sub>2</sub> to be etched. PBSG on the top followed by PECVD SiO<sub>2</sub> just above the MEMS and thermal SiO<sub>2</sub> below the MEMS (See Figure 4.1 (d)). With a positive resist mask of 2  $\mu$ m AZ 5214E, a combination of dry and wet etch was done. The rationale behind the choice is a difference in the wet etch rates for the three types of SiO<sub>2</sub>.

The etch rate for PBSG, thermal SiO<sub>2</sub> and PECVD SiO<sub>2</sub> in bHF was found to be widely different (approx. 45 nm/min, 70 nm/min, and 147 nm/min respectively for relatively open etch areas). Just bHF etch would have translated to etch time of more than 30 min which was not desirable for the resist mask. Thus, the etch was completed in a combination of dry and wet etching. The dry etch rates for PECVD SiO<sub>2</sub> and PBSG in the ICP chamber at Danchip were similar ( $\sim$  250 nm/min). So, dry etch was used to etch through PBSG and stop with a thin layer of PECVD SiO<sub>2</sub> (200 nm) left unetched (Figure 4.6). The remaining PECVD SiO<sub>2</sub> and thermal SiO<sub>2</sub> below MEMS were then etched away in bHF. Etch time for bHF wet etching was reduced to around 18 min (with 2-3 min of over-etch).

#### 4.1.3.3 *Resist Strip*

At this point, it was crucial not to remove the sample from the liquid interface. The buried oxide under the MEMS was etched away. So, bringing it out would result in MEMS sticking to the substrate and possibly breaking. So, care was taken to ensure proper han-



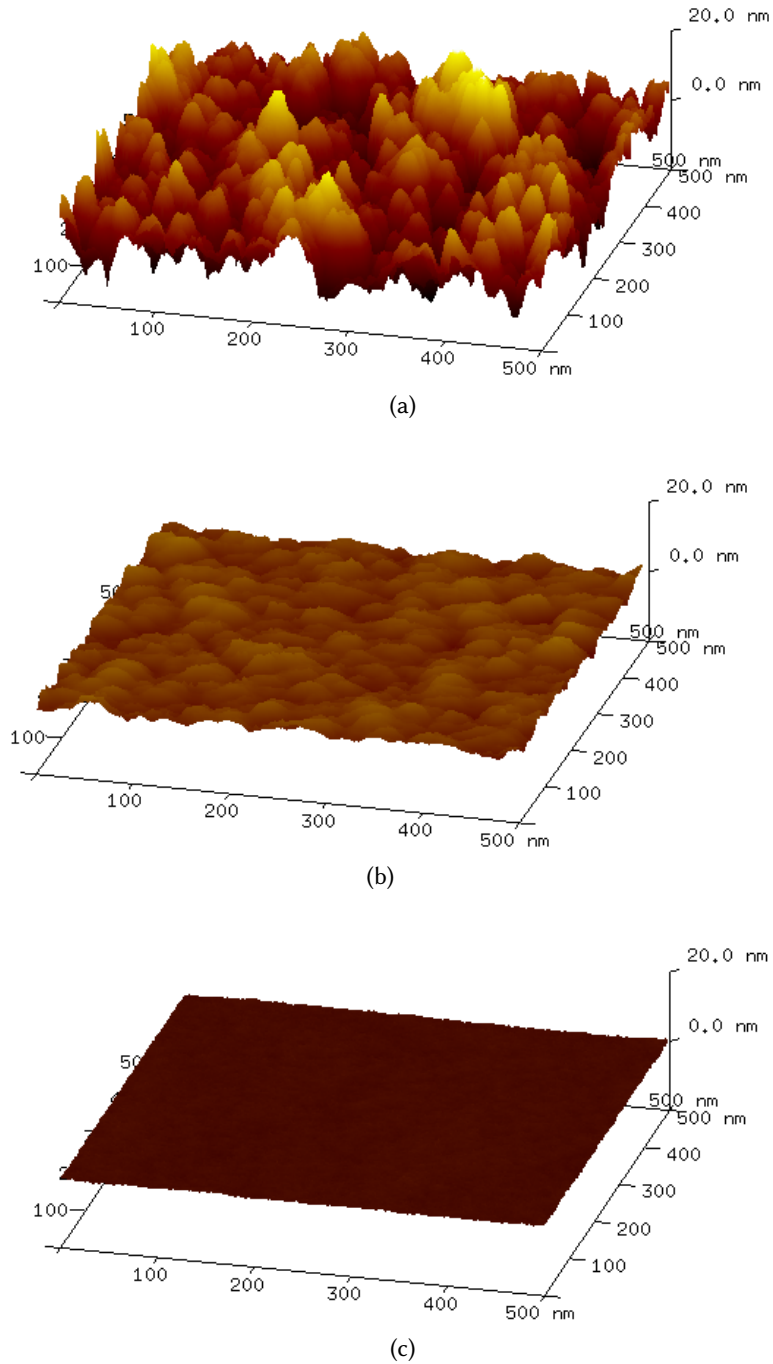


Figure 4.5: AFM Images showing the surface roughness (Average Roughness,  $R_q$ ) of (a) PECVD  $\text{SiO}_2$  (4.48 nm), (b) LPCVD TEOS (1.06 nm) and (c) PECVD  $\text{SiO}_2$  (0.18 nm) with an addition of PBSG and annealed at 1000 °C. Please note that the z axis has been kept the same for all the images to show the difference in surface quality.

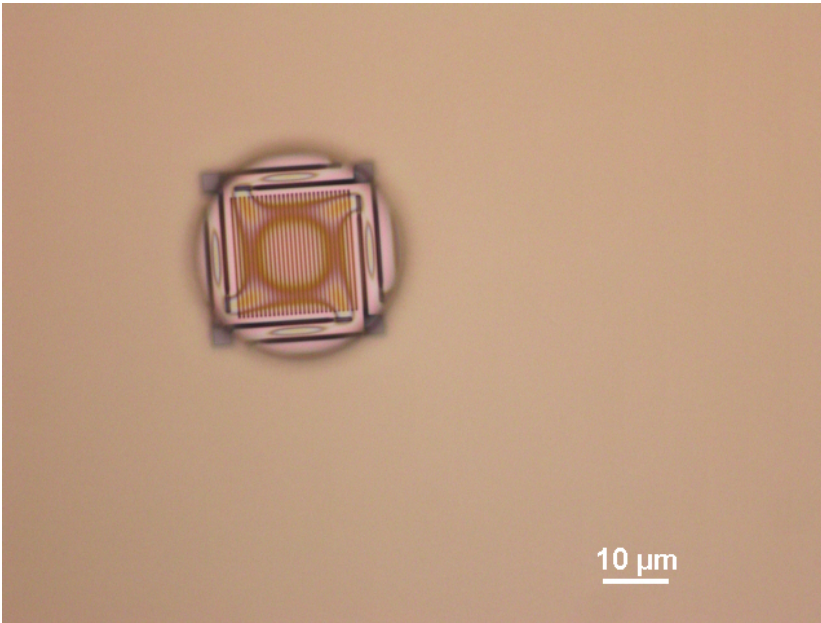


Figure 4.6: Microscope image of the device after a dry etch of  $\text{SiO}_2$ .

dling and make all transfers with the sample submerged in liquid. So, bHF was exchanged with water for rinsing, followed by ethanol to remove water and finally acetone to strip the resist mask. Appendix A.6 outlines the complete handling protocol.

#### 4.1.3.4 CPD Release

To successfully release the MEMS, the sample had to be kept in a liquid with low surface tension followed by heating to evaporate the liquid. A commercial critical point drying (CPD) was used for this. In the CPD chamber, the sample was first placed in isopropyl alcohol (IPA), which was eventually replaced with liquid carbon-dioxide at a low temperature of 10 °C. Later, the chamber was heated under pressure (40 °C, 1400 psi) to evaporate  $\text{CO}_2$ . At this temperature and pressure, the  $\text{CO}_2$  exists as a mixture of liquid and gaseous phase. Bringing down the pressure at 40 °C then converts all of the  $\text{CO}_2$  to gaseous phase and thus prevents sticking of the MEMS.

An alternate method to do this was to etch thermal  $\text{SiO}_2$  in HF vapor. However, some basic tests showed that vapor etch process-

ing required a great amount of control on the set-up, gas flow and needed special handling to ensure safety. Further, the reaction for the etch is initiated by the water on the sample surface and one of the by-products of the reaction is also water [10, 73], which defeats the purpose of using vapor to release MEMS (while avoiding high surface tension liquid). So, it was not pursued further.

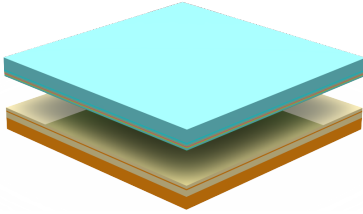
## 4.2 PHASE II: BONDING AND CONTACT DEFINITION

This phase (Figure 4.7) covers the bonding of processed SOI from the previous phase with an InP wafer containing QWs. Processing of the bonded sample to define the contact regions is also discussed in this phase.

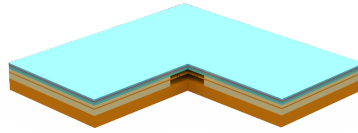
### 4.2.1 *Active Material*

Active material (QWs) for 1550 nm MEMS VCSEL was grown on an InP wafer (with a surface roughness of around 0.2 nm). QW and barrier were defined by indium gallium arsenide phosphide (InGaAsP) and indium gallium aluminium arsenide (InGaAlAs) respectively. There were in total 8 QW layers grown for this run (Figure 4.9). The active material was sandwiched by InP on both sides. The placement of QWs inside InP was decided based on the simulations (Section 2.3.3) so as to have maximum overlap (confinement factor) with the electric field. Refer Appendix A.3 for more information on the complete growth stack.

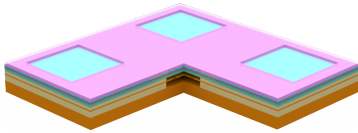
The QWs are directly responsible for the gain achieved in a laser cavity. So, in principle, growing a large number of QW layers would help. However, the growth of QWs is tricky and heating from absorption is also proportional to the number of wells. QW layers are strained and increase in the number of layers may lead to increase in defects. This leads to non-radiative recombination which will prevent large carrier densities and thus broadband gain. So, QWs grown for this run have been optimized to fit one antinode of the field and reduce defects in the layers. As an improvement over the current design, QWs can be designed to span over a range of wave-



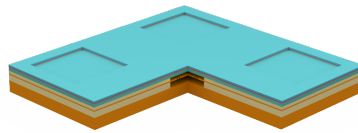
(a) Low temperature bonding of SOI wafer with InP wafer, using 2 nm of ALD  $\text{Al}_2\text{O}_3$  as the intermediate layer



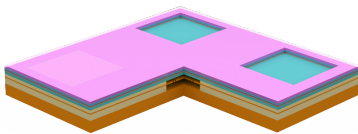
(b) InP substrate etch



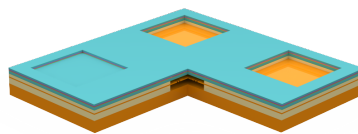
(c) Resist mask for etch to the n-doped InP layer



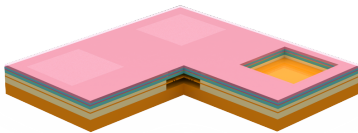
(d) After etch to the n-doped InP layer



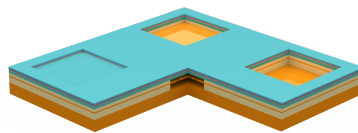
(e) Resist mask for etch to the Si MEMS layer



(f) After etch to the Si MEMS layer

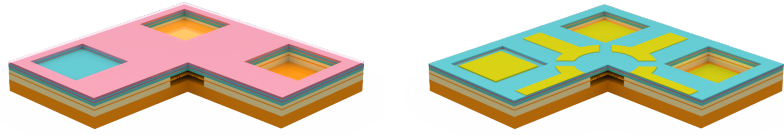


(g) Resist mask for etch to the Si substrate



(h) After etch to the Si substrate

Figure 4.7: Phase II fabrication steps



(a) Mask for depositing metal stack for (b) Metal contact deposition with heat-contacts. A variation of this mask includes heat pads as shown in 4.8 b

Figure 4.8: Phase II fabrication steps (continued)

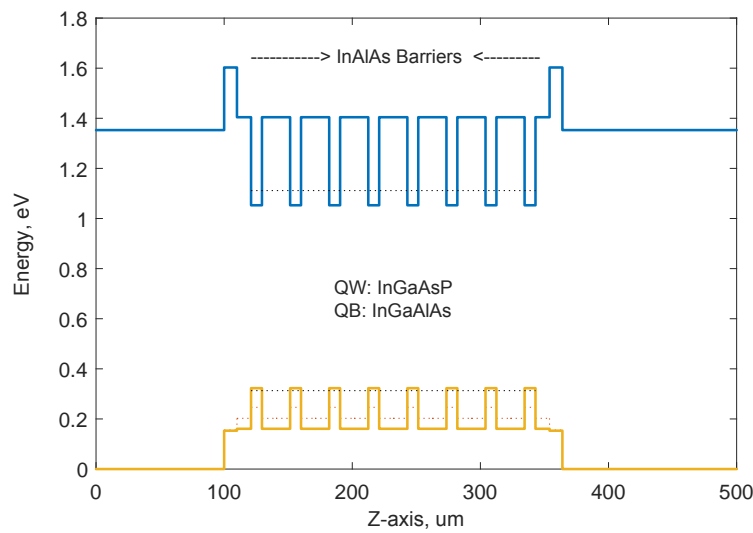


Figure 4.9: Band diagram of the gain region showing QWs and barriers.

lengths, which will lead to a broader bandwidth of gain spectrum. More on this will be discussed in the future outlook (Chapter 6).

#### 4.2.2 *Bonding*

The InP wafer with grown active material was then bonded to the processed SOI wafer from Phase I, using low-temperature direct bonding using Al<sub>2</sub>O<sub>3</sub> as the intermediate layer (3.3.4). The bonded wafers were then annealed at 300 °C. (See Appendix A.7 for more details.)

Handling of the wafers was very critical until this point. It was important to avoid any particles or contamination which could have resulted in voids/un-bonded regions. So, all the processing steps until this point were optimized to minimize particle contamination. This was also the reason for bonding a full InP wafer instead of bonding pieces. From here on, the sample was less sensitive to particles.

#### 4.2.3 *Contact Definition*

After annealing, the InP substrate was etched away (Figure 4.10) and a thin layer of InP containing QWs was left behind (Figure 4.11). Only the bonded layers survive a substrate etch, which makes this a qualitative test for all the processing done until this point. In our run, we had a yield of approx. 60%. The sample was then cleaved into four parts. This was essential as the masks for the next steps were designed for 1-inch squares.

There were three set of etches to be done in order to reach the different actuation electrode layers: n-doped InP (top electrode), Si MEMS layer (centre electrode) and the silicon substrate (bottom electrode).

##### 4.2.3.1 *Etch to doped InP*

The first set of etches was to reach the n-doped InP layer, below QWs (Refer the growth sheet A.3). The mask was defined using

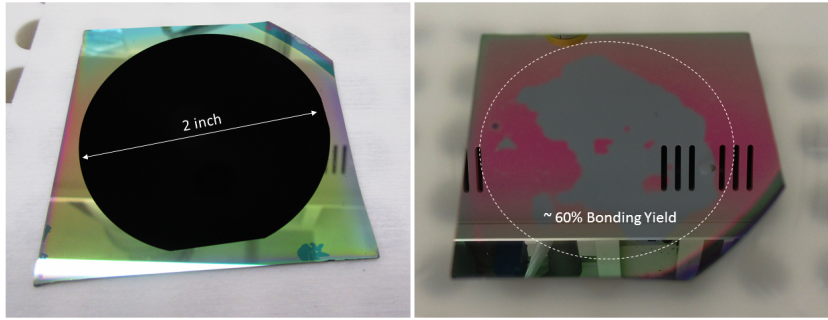


Figure 4.10: A 2-inch InP wafer bonded to quarter of 6 inch SOI wafer and  $\text{Al}_2\text{O}_3$  dry etched. (Left) Before substrate removal. (Right) Bonded InP after complete substrate removal.

$\text{SiO}_2$  (hard mask) and resist. The  $\text{SiO}_2$  hard mask was essential to address poor adhesion between InP and resist. Layers etched in this step were InP and QWs. The resist mask could have been removed as a  $\text{SiO}_2$  mask was enough. A combination of dry (for InP) and wet etching (for QWs) was used for the etch.

A dry etch for both layers would have damaged the n-doped layer from ion bombardment and a wet etch alone would have meant losing control of the etch profile. A combination of both gave the best result. Dry etching was used to etch the InP till the QWs and a selective wet etch was used for etching away the QWs. (See Appendix A.9 for more details.) This reasoning was also followed in rest of the etches for defining the contacts, in order to avoid damages to the contact surfaces.

Both the masks were removed at the end of the etches. The device after the etch is shown in Figure 4.12.

#### 4.2.3.2 Etch to SOI device layer

The second set of etches established contacts to the Si MEMS layer. Similar to the previous etch, a mask was defined using  $\text{SiO}_2$  and resist. Layers etched were the remaining InP layer below QWs, 2 nm  $\text{Al}_2\text{O}_3$  from bonding interface and the spacer layer  $\text{SiO}_2$ .

A combination of dry and wet etches was also used here. InP and  $\text{Al}_2\text{O}_3$  were dry etched on RIE and ICP system respectively. (This was simply due to existing recipes on the two systems.) 90% of

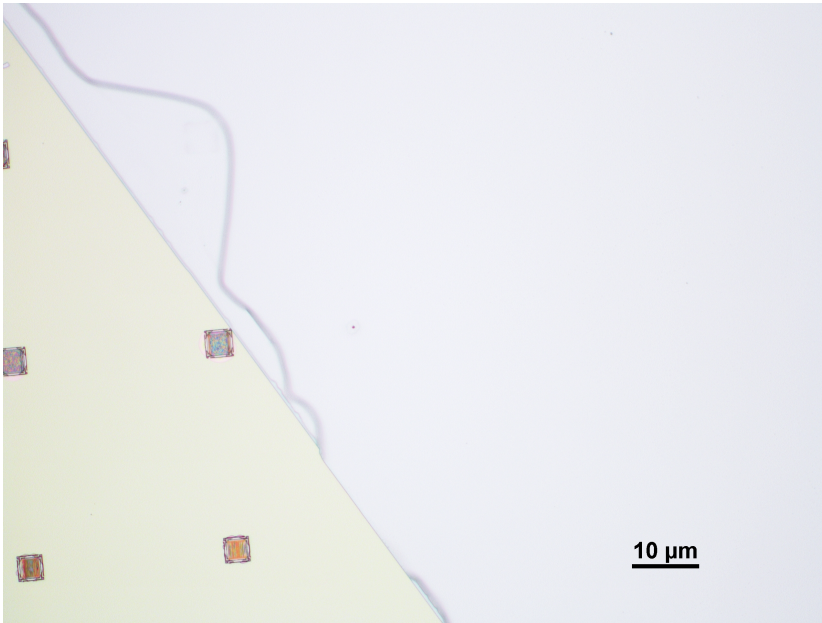


Figure 4.11: Microscope image showing boundary of the bonded region. Underlying MEMS structure is visible in the un-bonded region on the left.

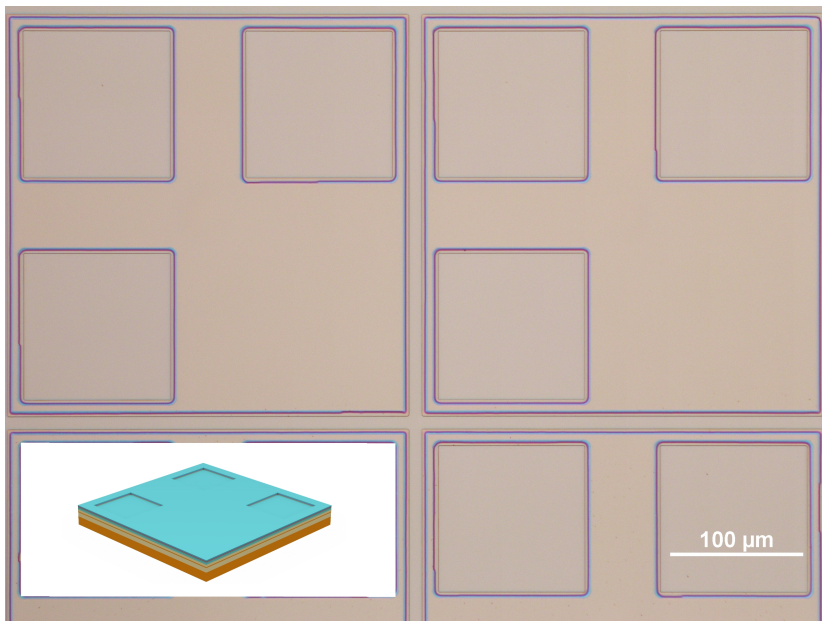


Figure 4.12: Microscope image after the completion of etches to n-doped InP.



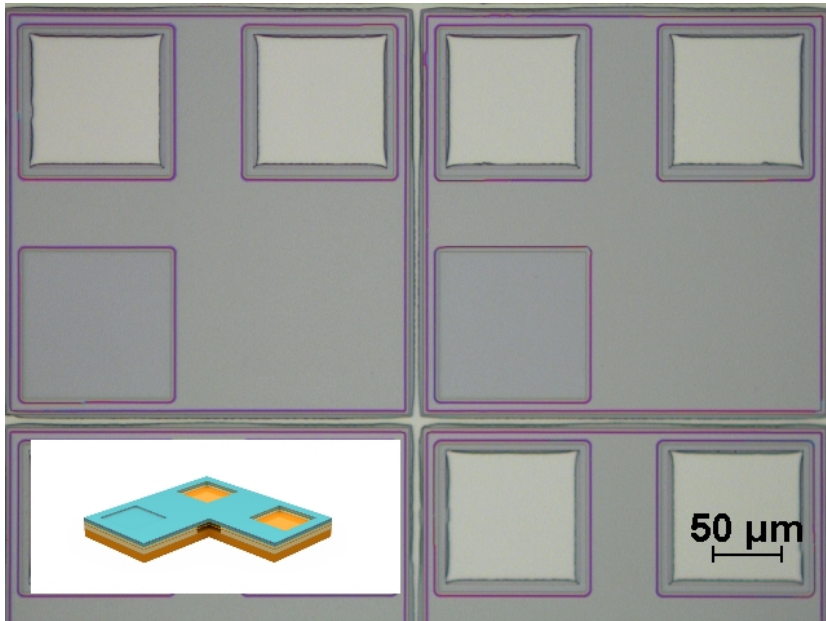


Figure 4.13: Microscope image after the completion of etches to silicon MEMS layer.

the spacer layer was etched by RIE with just 100-150 nm of  $\text{SiO}_2$  remaining on top of the Si MEMS layer, which was then removed by bHF. (More details in Appendix A.10.) The etched pattern is shown in Figure 4.13.

Resist mask was essential here for the dry  $\text{SiO}_2$  etch. So, if there was any damage in the resist profile, during the first two dry etches, the resist mask was ashed and re-patterned for the  $\text{SiO}_2$  etch.

#### 4.2.3.3 Etch to Silicon substrate

The last group of etches was used to define an opening to the Si substrate. A combination mask of  $\text{SiO}_2$  and resist was also defined here. Layers etched were Si MEMS layer and buried oxide (thermal  $\text{SiO}_2$ ).

The Si layer was dry etched and thermal  $\text{SiO}_2$  was etched in two steps: dry etch until 100-150 nm unetched  $\text{SiO}_2$ , which was etched by bHF etch (Figure 4.14). See Appendix A.11 for details.

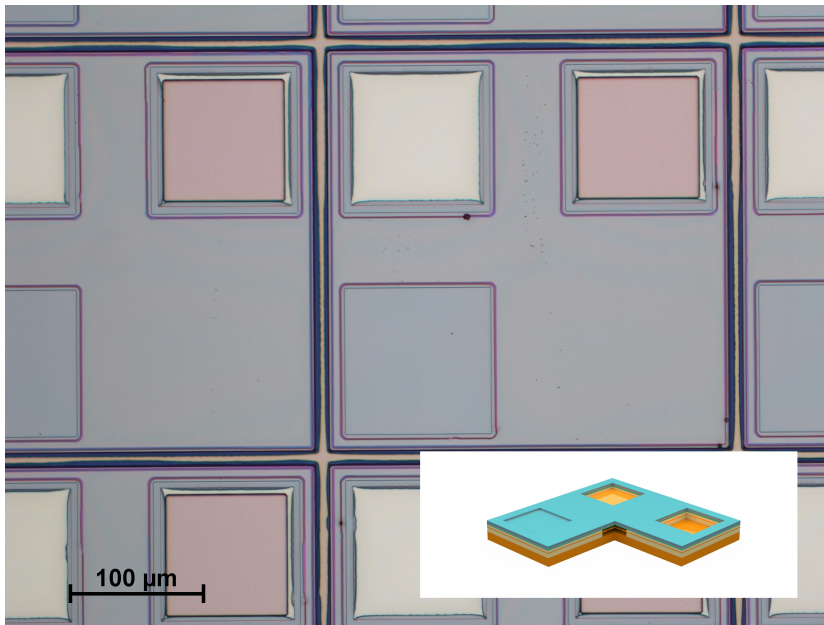


Figure 4.14: Microscope image after the completion of etches to the Si substrate.

#### 4.2.3.4 *Metal Deposition*

After etching through the bonded stack to the desired contact layers, metal was deposited to establish ohmic contact for MEMS electrostatic actuation.

AZ nLOF 2070 negative resist (best choice for liftoff process) was used as the mask for depositing the metal stack. Owing to low adhesion of resist to InP,  $\text{SiO}_2$  was also used as a hard mask here. The metal stack (25 nm titanium + 75 nm platinum + 300 nm gold) was deposited in an evaporation system. (More information in Appendix A.12) and liftoff was done in acetone (Figure 4.15). The metal stack chosen for this run was not optimized for contact to n-InP layer. This will need to be optimized for any future runs.

The  $\text{SiO}_2$  layer used as mask above (the dark brown region in Figure 4.15) was deposited using PECVD and this was not removed at the end of the process. It served as the first layer for the DBR structure. The DBR will be defined by a sputtering system which might create damage on the top of InP and thus give non-radiative

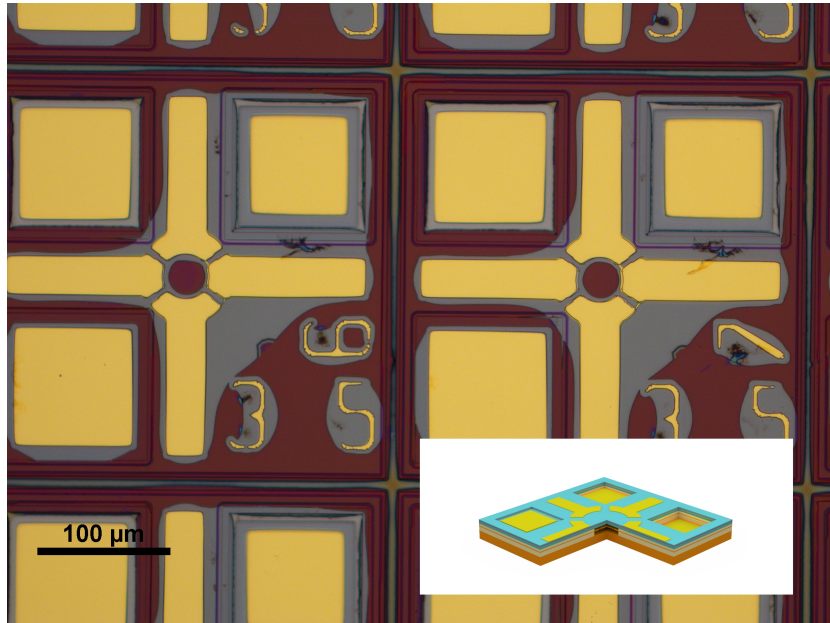


Figure 4.15: Microscope image after the metal stack deposition and liftoff process. The grey region seen in the image is the exposed InP layer due to an over etch of the SiO<sub>2</sub> mask (dark brown region). It was caused due improper adhesion with the resist.

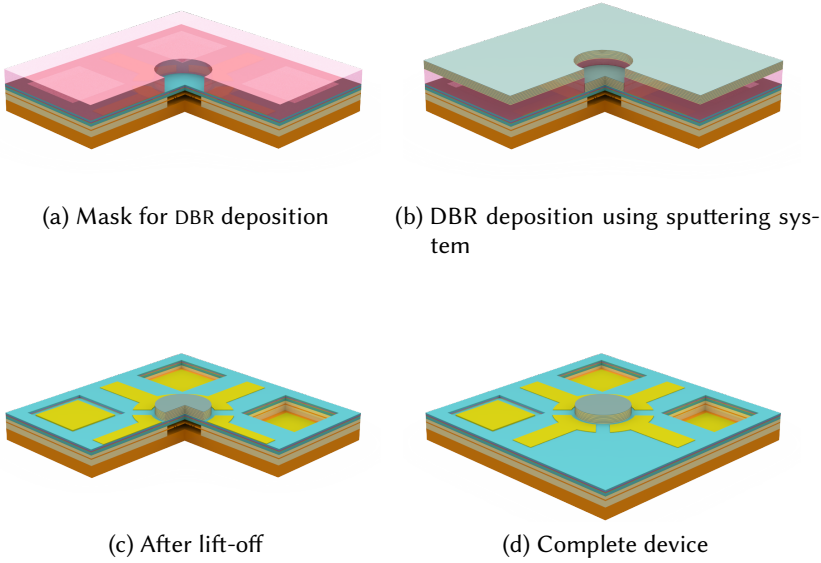


Figure 4.16: Phase III fabrication steps

recombination, poor contacts and even add optical losses. So, having a protection layer helps avoid that.

### 4.3 PHASE III: DBR DEPOSITION

The next and the last leg of the fabrication was the top dielectric mirror deposition as shown in Figure 4.16. High refractive index  $\text{TiO}_2$  (2.31 at 1550 nm) and low refractive index  $\text{SiO}_2$  (1.44 at 1550 nm) pair was chosen for the top dielectric mirror.

To achieve high reflectivity, 7 pairs of  $\text{TiO}_2$  and  $\text{SiO}_2$  were chosen and each layer thickness was further optimized to retain high reflectivity around 1550 nm while having a small reflectivity around the pump wavelengths - 980 nm and 1310 nm (Section 2.3.1).

7  $\mu\text{m}$  AZ nlof 2070 negative resist mask was used to define circular openings centred around the device. The mirror stack was deposited using a sputtering system. Lift-off was done by Remover 1165 at 60 °C. Figure 4.17 shows the device after liftoff. (See Ap-

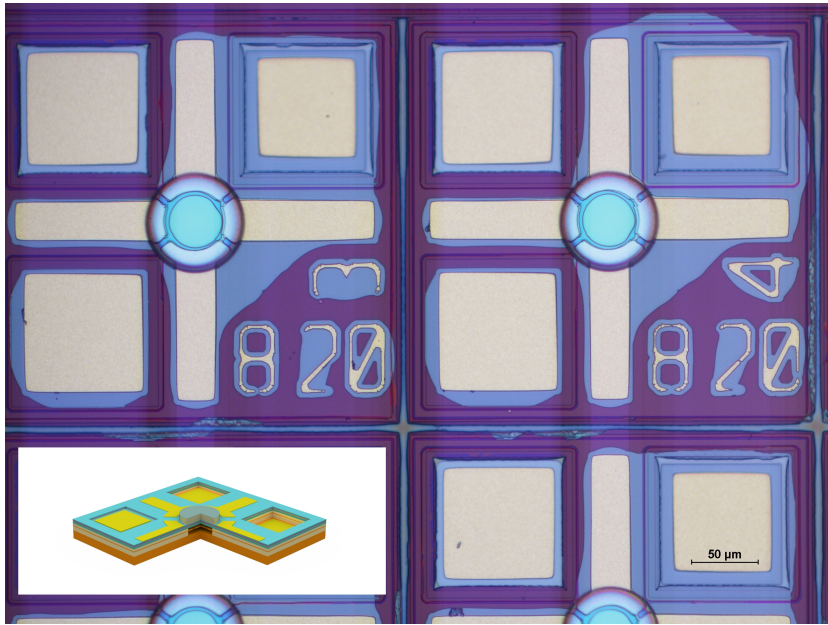


Figure 4.17: Microscope image of the device complete with dielectric DBR mirror.

pendix A.13 for more information about the thicknesses of individual layers.)

The mirror deposition for this run was done at the fabrication facility of Chalmers University, Sweden. The choice to perform the mirror deposition at an external facility was driven by unexpected breakdowns of deposition systems at DTU Danchip. The deposition recipe with optimizations was developed earlier on dielectric- evaporation system and ion beam assisted sputter deposition (Appendix A.15) but unfortunately, could not be used.

#### 4.4 SUMMARY

A 1550 nm tunable MEMS VCSEL was fabricated (Figure 4.18). Many challenges were addressed while designing the fabrication process flow. The major being development and integration of a wide range of fabrication processes into a single process flow, which encompassed standard processing like - Si etch, SiO<sub>2</sub> deposition, annealing, CPD, III-V etching, metal deposition, dielectric deposition etc.

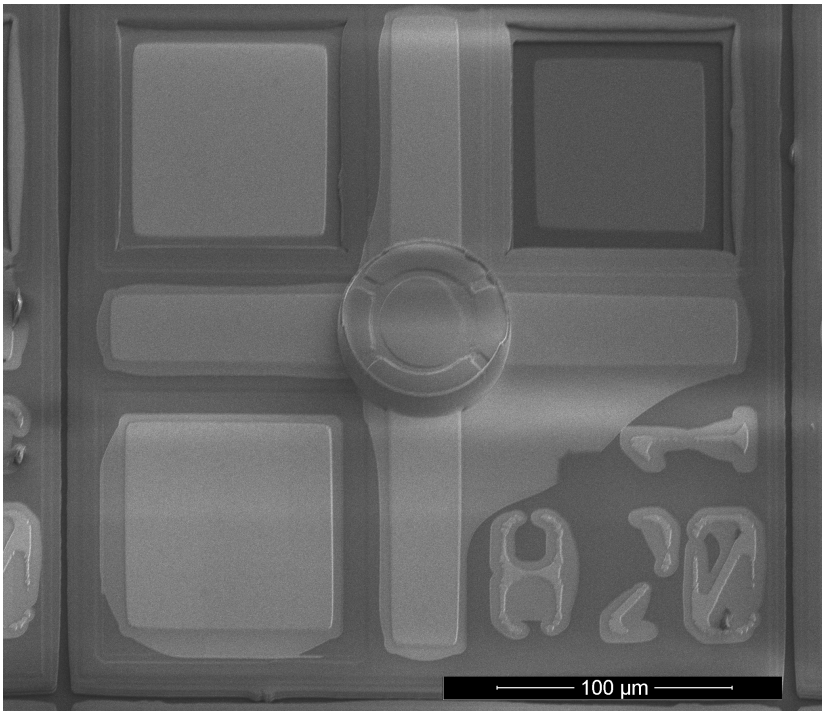


Figure 4.18: SEM image of the fabricated device.

and non-standard processing like PBSC deposition for low surface roughness and the integration of InP with SiO<sub>2</sub>. In addition, availability, reliability, and reproducibility of fabrication tools brought challenges in understanding processes. Dividing the fabrication process into separate phases was helpful in debugging issues and developing processes. As mentioned in the chapter, there is a lot of room for improvement for any future runs.

Despite the challenges, the developed fabrication process flow brings in a lot of flexibility from a design perspective. Any changes in the design wavelength or tuning requirements would require minor changes in processing parameters, without any major process change. So, it is easy to accommodate any required changes in the design (be it the lasing wavelength or the III-V material or the tuning mechanism).

The characterization of the device is discussed in the next chapter.

## Part III

# THE ACCOMPLISHMENT





## CHARACTERIZATION

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Characterization is the final test for all the hard work that went into the design and fabrication of the proposed microelectromechanical systems (MEMS) vertical-cavity surface-emitting laser (VCSEL). This project was aimed at realizing a proof-of-concept device for the proposed design. So, the primary goal of this thesis is to achieve lasing and a wide enough ( $> 50$  nm) tuning range. In future, optimization in the design and fabrication will ensure top performance, comparable to the state of the art.

This chapter, first, presents the optical setups and pump lasers used for characterization. Next, it presents the basic characteristics of a wavelength tunable laser, which includes both DC and AC voltage tuning. The chapter then covers the discussion on thermal effects on the device and finally concludes with a brief discussion on the issues in the fabricated device.

### 5.1 SETUP

A simple microscope-based optical setup was used for characterizing the fabricated MEMS VCSEL. Commercially available laser diodes: 980 nm and 1310 nm, were used as the pump sources. A near-infrared (NIR) camera mounted on top of a microscope was used for looking at the sample and position the pump beam. The laser output was collected on an optical spectrum analyzer (OSA), which was further connected to a NI GPIB system for data collection and analysis on a computer. There were three types of the setups, with small variations, used for the characterization process.

### 5.1.1 Basic Setup

Figure 5.1 illustrates a schematic of the optical setup for the MEMS VCSEL characterization. In this setup, the pump laser and the MEMS VCSEL laser output share most of the optical path. A laser diode (either 980 nm/ 1310 nm) was used as the pump source. The light from the source was fed through an optical fiber into a microscope with the help of a piezo stage and a collimating lens. The piezo stage helped in positioning and alignment of the pump beam. The pump beam was then directed at the sample using a dichroic mirror at 45 degrees and focusing objective lens (either 20X and 50X). The sample was placed on a 2D translation stage, which had a vacuum holder and was temperature controlled. The laser output from the fabricated device was collected back the same way, through the objective lens, dichroic mirror and the piezo stage into the optical fiber. A wavelength-division multiplexer (WDM) coupler [99] was used between the pump laser and piezo stage to filter out the 1550 nm component (MEMS VCSEL laser output). It was then connected to an OSA. A part of the output was also used as a feedback for optimal positioning the fiber at the back of the microscope. Inside the microscope, a small fraction of the MEMS VCSEL output was transmitted through the dichroic mirror. It was filtered using a longpass 1310 nm filter to just look at the MEMS VCSEL output using a NIR camera. It was helpful in quick scanning through the fabricated chip and manual positioning of the pump beam and probes.

The input and output spectra shared the same optical components, which may or may not be optimal for both. The pump and lasing wavelengths are wide apart in the spectrum which makes it a challenge to design low loss optics for all operating wavelengths. The losses in the objective lens, in particular was hugely dependent on the wavelength.

#### 5.1.1.1 Losses

The lens used for the microscope were Mitutoyo's NIR infinity corrected objective lenses<sup>1</sup> [1, 2]. These were unfortunately not optimal for both pumping and laser collection wavelength regimes. At

<sup>1</sup> The 20X objective lens used in the characterization is optimized for 1060 nm and the 50X objective is optimized for the NIR region.

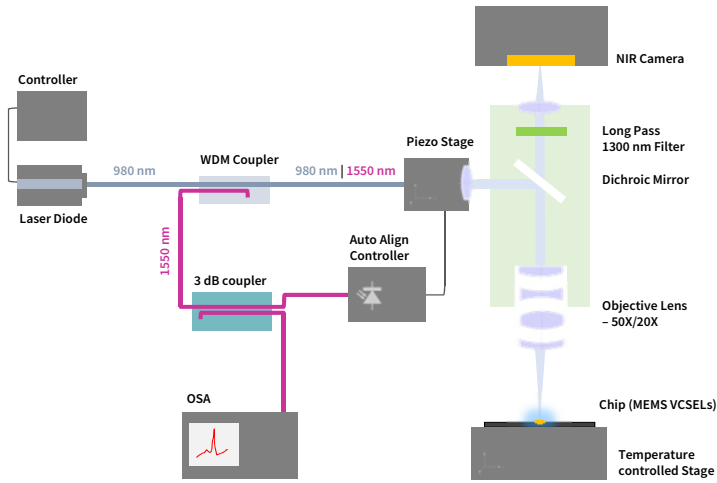


Figure 5.1: Illustration of the characterization setup using a 980 nm laser for pumping. It can also be used for a 1310 nm pump laser. A microscope based setup was used for the pumping and collection of lasing light. A NIR camera was added on the top of the microscope to look and position the sample. (Setup1)

980 nm, the losses were around -2 dB and -4 dB for 20X and 50X objectives respectively. i.e., only approximately half of the 980 nm pump power is lost at the objectives. 50X had more glass/lens interfaces which accounted for the extra loss over 20X. The loss was even worse for higher wavelengths. At 1550 nm, the losses were -5 dB and -8 dB for 20X and 50X respectively. The collection losses were not quite as troublesome as they could be corrected later for the loss. However, pump laser diodes had finite output power and losses in the optics would limit the delivered power onto the chip. So, two alternate setups were considered to work around the objectives.

### 5.1.2 *Probe Setup*

Two variations of the basic setup (Figure 5.2 and 5.3) were also used for characterization. In these setups, the pump laser was guided through an alternate path in order to avoid the high losses in the microscope setup. For pumping, the pump source was connected directly to an optical probe which was placed close to the sample, just below the microscope objective. It consisted of a small 1X focusing lens pair and a short pass 950 nm dichroic mirror [97] at 45 degrees. The dichroic mirror reflected around 95% of the MEMS VCSEL laser output and allowed the rest to go through the microscope. In Setup2, the lasing spectrum was collected in a similar manner to Setup1, through the microscope. In Setup3, a WDM coupler is added after the pump source, which separated the lasing spectrum from the pump. The microscope was essential in both the setups for visual placement of the pump beam on the chip.

## 5.2 PUMP LASER

Commercial laser diodes from Thor labs (976nm [96] and 1310nm [98]) were used as the pump lasers. The maximum power output obtainable on the 976 nm and 1310 lasers are 350 mW and 130 mW<sup>2</sup> respectively. The pump lasers were first characterized to determine the actual power delivered on the chip after all the losses in the

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<sup>2</sup> The maximum power for 1310 nm laser diode degraded during the characterization process to 70 mW

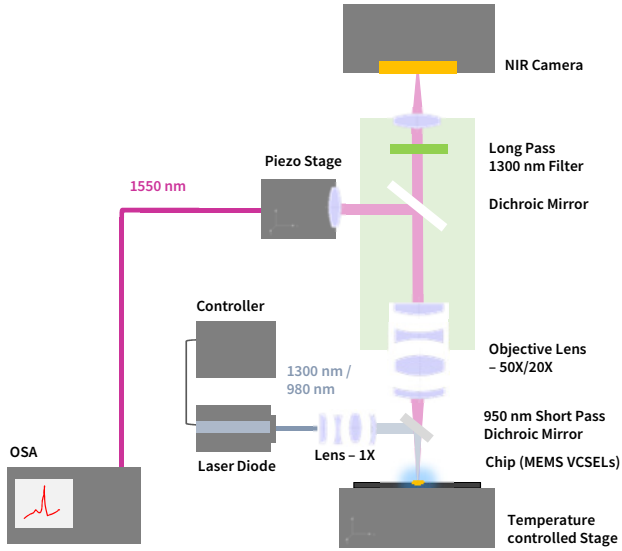


Figure 5.2: Illustration of the characterization setup using a probe for pumping and microscope for collection. Microscope with a NIR camera was used for sample positioning. (Setup2)

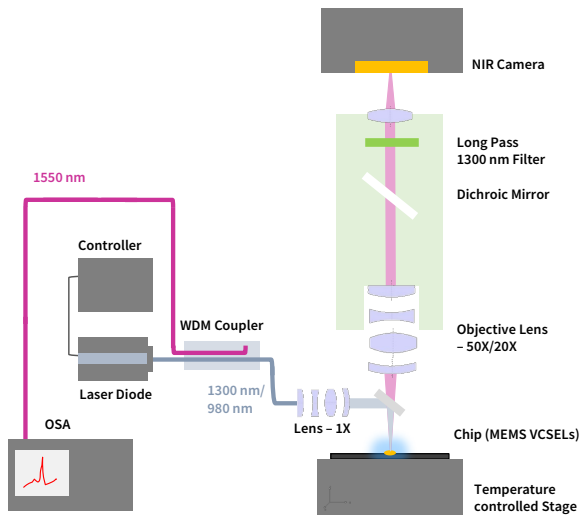


Figure 5.3: Illustration of the characterization setup using a probe for pumping and collection. Microscope with a NIR camera was used for sample positioning. (Setup3)

setup. The pump spot was also important for mode definition as discussed earlier in section 2.3.4. So the spot size of the pump beam was also characterized. All the measurements in this section were done on Setup1.

### 5.2.1 *Efficiency*

The amount of power delivered on the chip is dependent on the pump laser power and the losses incurred by the laser. The pump power was controlled using pump laser current on the laser diode controller. On the other hand, the total losses in the system is a combination of losses from connectors, optical fibres, WDM coupler, alignment stage, dichroic mirror and most importantly objective lenses. In this study, the losses in the objective lens was much higher than other sources. So, it is the only variable for this discussion. The loss is also dependent on the operating wavelength. So, it varied based on the wavelength and optics in use. Figure 5.4 shows the power collected under the microscope objective for variations in pump laser current and the objective lens. There are two important conclusions to derive from the obtained data. First, the 1310 nm laser delivered substantially lower power to the chip compared to the 980 nm laser in Setup1. Second, 50X was lossier than 20X as expected, and the effect was more profound for the 980 nm laser compared to 1310 nm. Even so, a maximum of 160 and 80 mW was delivered using the 980 nm laser with 20X and 50X lenses, respectively. In contrast, only a maximum of 30 mW was available for the 1310 nm laser (for both 20X and 50X objectives). Over all, the total losses in Setup1 using a 980 nm laser were -3.4 and -6.4 dB for 20X and 50X receptively. Similarly, the losses in the same setup for 1310 nm pump laser was -6.4 dB for both the objective lenses.

Considering the low available power and high losses in the case of a 1310 nm pump laser for Setup1, only 980nm pump laser was used for Setup1.

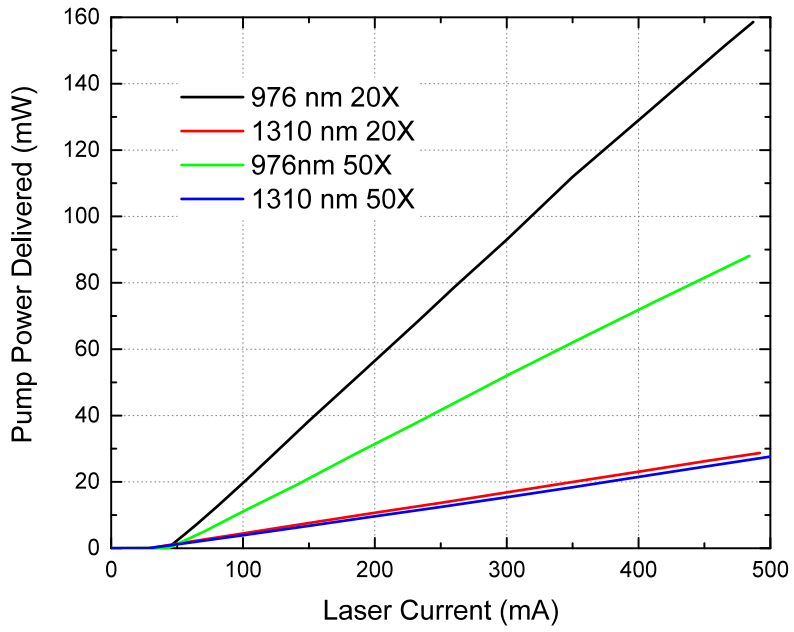


Figure 5.4: Amount of power delivered on top of the chip using Setup1 for 980 nm and 1310 nm lasers with 20X and 50X magnification lenses.



### 5.2.2 Mode Size

The optical pump profile has a direct influence on the lasing mode. Ideally, the pump beam should have a Gaussian beam profile with a beam width ( $1/e^2$ ) around  $8\ \mu\text{m}$  for single mode lasing.

To look at the pump beam profile, it was focused on the chip where there were no devices but a blanket layer of InP (with QWs) on top of spacer  $\text{SiO}_2$ . The spontaneous emission from that region was imaged using NIR camera. (Figure 5.5) The integration time on the NIR camera was then adjusted so as not to saturate the signal. Adjustments were also made on the piezo stage, connected at the back of the microscope, to ensure a circular pump spot. The focus of the spot was also adjusted when the objective was changed.

Figure 5.6 and 5.7 show the transverse profile of the spontaneous emission from the pump beam spot with 50X and 20X objective respectively. A smaller spot with  $1/e^2$  width of  $9.7\ \mu\text{m}$  (full width at half maximum (FWHM) :  $5.7\ \mu\text{m}$ ) was achieved for a 50X objective, which is closer to our calculations for single mode lasing. So, 50X objective with 980 nm on Setup1 was used as the primary arrangement, unless mentioned, for the next characterization measurements.

### 5.2.3 Absorption

The amount of pump power absorbed in the active layer is also an important factor in making a choice for the pump wavelength and power. Absorption is dependent on the band structure of the materials in the grown active layers (Figure 4.9). 980 nm pump laser will get absorbed both in the QWs and the barriers. Assuming an absorption coefficient of  $10^4\ \text{cm}^{-1}$ , the total power absorbed by 296 nm of active material is around 25 %. Similarly, for 1310 nm pump laser, the absorption will only occur at the QWs. Unlike 980 nm, the absorption is dependent on the number of states available. Assuming with 1310 nm pumping we can access just one state per quantum well, the total absorbed power is around 8% (1% per QW [15]). Thus, a 980 nm laser is three times more effective than 1300 nm laser. At the same time, 980 nm laser gets absorbed by Si, which

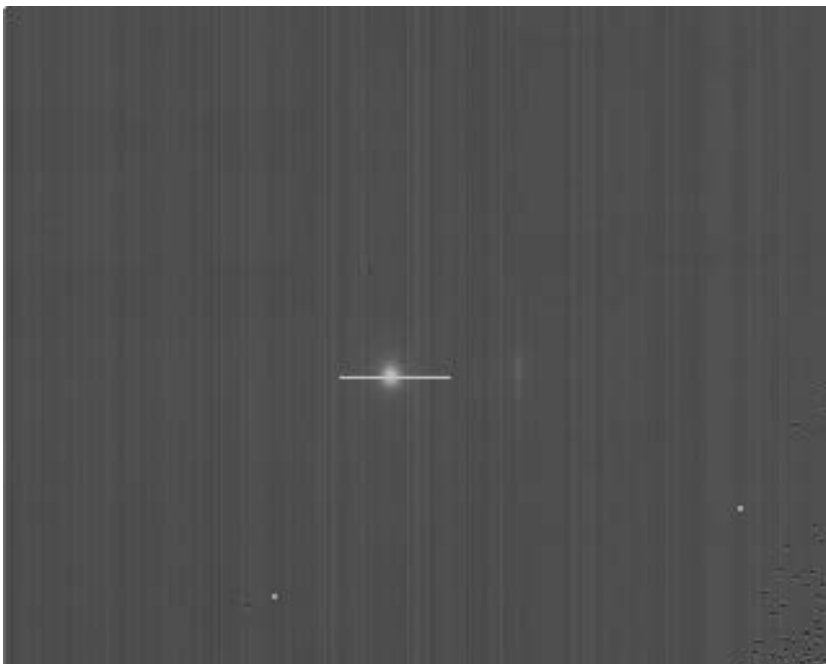


Figure 5.5: Grayscale image showing spontaneous emission when 980 nm pump laser is positioned on top of InP layer with active layers (with no device beneath).

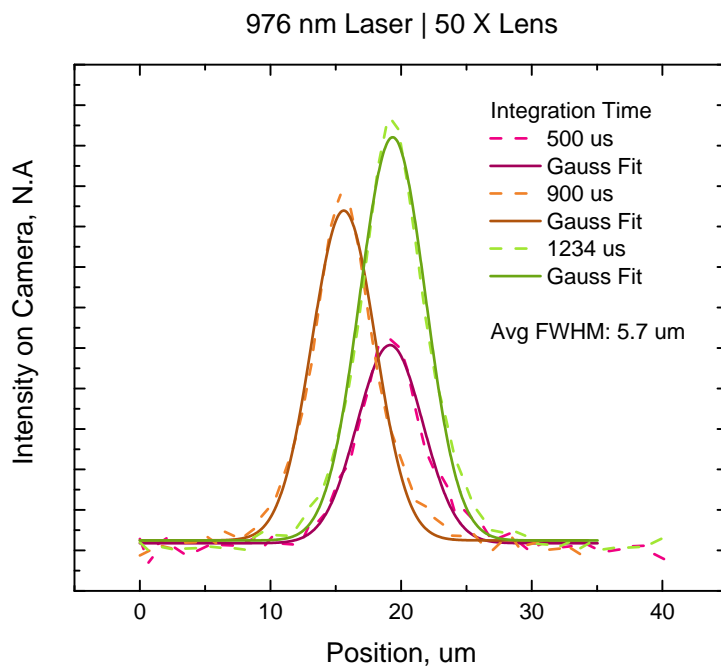


Figure 5.6: Approximate pumping mode shape (pumping spot size) obtained for a 980 nm pump laser for different integration time. An average FWHM width of 5.7  $\mu\text{m}$  was obtained with the 50X magnification lens.

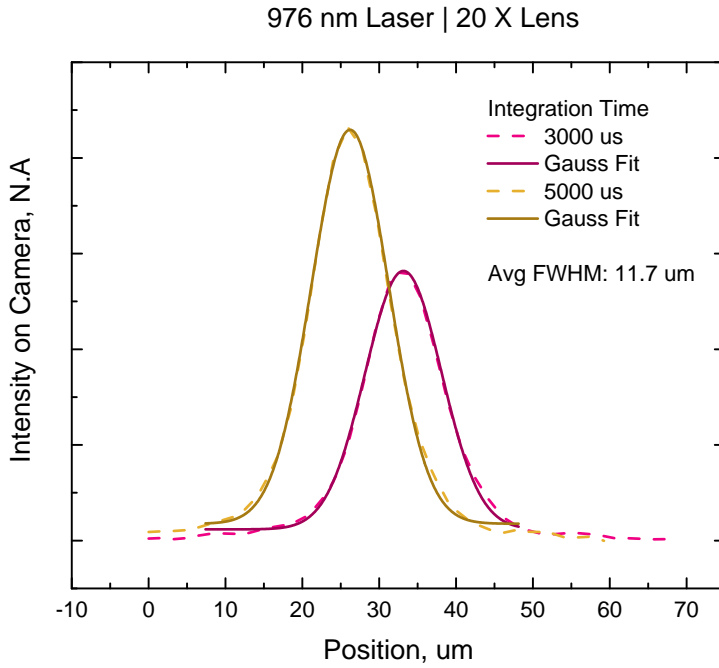


Figure 5.7: Approximate pumping mode shape (pumping spot size) obtained for a 980 nm pump laser for different integration time. An average FWHM width of 11.7  $\mu\text{m}$  was obtained with the 20X magnification lens.

is the material for the HCG in the proposed design. So, it may induce unwanted heating of the Si membrane too.

### 5.3 LASING

A well-defined beam was positioned at the centre of the device and the pump laser current was adjusted to achieve lasing. Figure 5.8 shows the NIR image of the laser spot from the fabricated MEMS VCSEL. Slight adjustments on the focus of the microscope also had to be made for lasing. So, the required pump size was slightly bigger than that achieved by 50X objective. It can be inferred that a pump spot ( $1/e^2$ ) of around 10-11  $\mu\text{m}$  was required for lasing.

Figure 5.8 shows the NIR image of the laser spot from a MEMS VCSEL on the fabricated chip and Figure 5.9 shows the lasing spectrum as seen on OSA. The peak was centered at 1562 nm with a high side mode suppression ratio (SMSR) of approximately 60 dB. There is some deviation in the lasing wavelength from the design wavelength for the device in discussion. It comes from fabrication imperfections in the processing. Based on the deposition variation, thicknesses may vary across the wafer. This results in changing the total optical cavity length and we see deviation in the lasing wavelength.

#### 5.3.1 *Threshold*

The threshold for lasing on the fabricated MEMS VCSEL was obtained by plotting the peak lasing power of the spectra for different pump laser diode current values (Figure 5.10). The threshold input power (delivered on the chip) at room temperature for the laser was approximately 5.5 mW, which translates to around 1.4 mW of absorbed power (based on our assumption of 25% absorption for 980 nm pumping). This is equivalent to an electrical injection current of 1 mA, which is comparable to some well-designed VCSELs [7, 19, 20, 70, 71].

The maximum power output achieved for the device is approx. 0.1 mW (after correction of 12 dB loss). There are some small variations on the threshold graph from the standard curve. This was

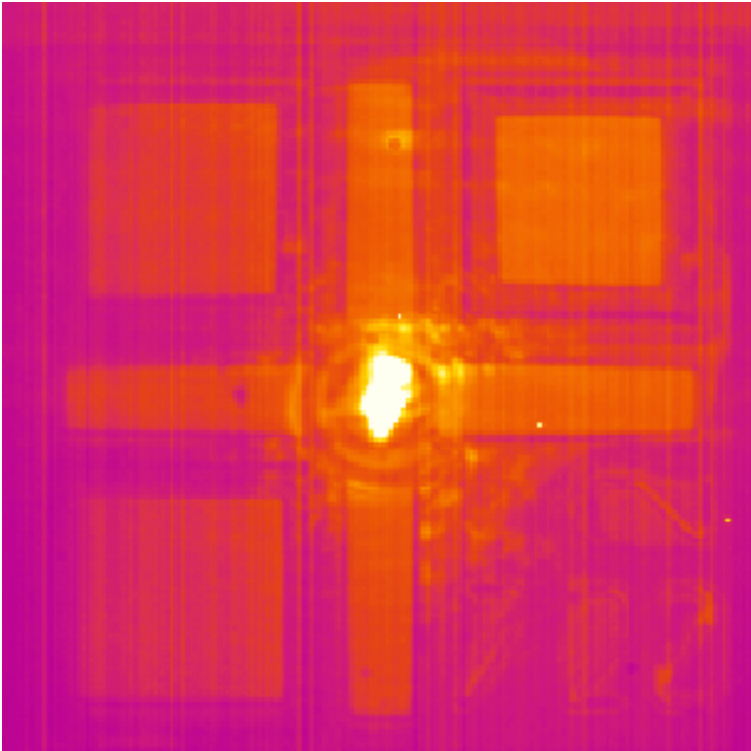


Figure 5.8: NIR image of lasing MEMS VCSEL using optical pumping.

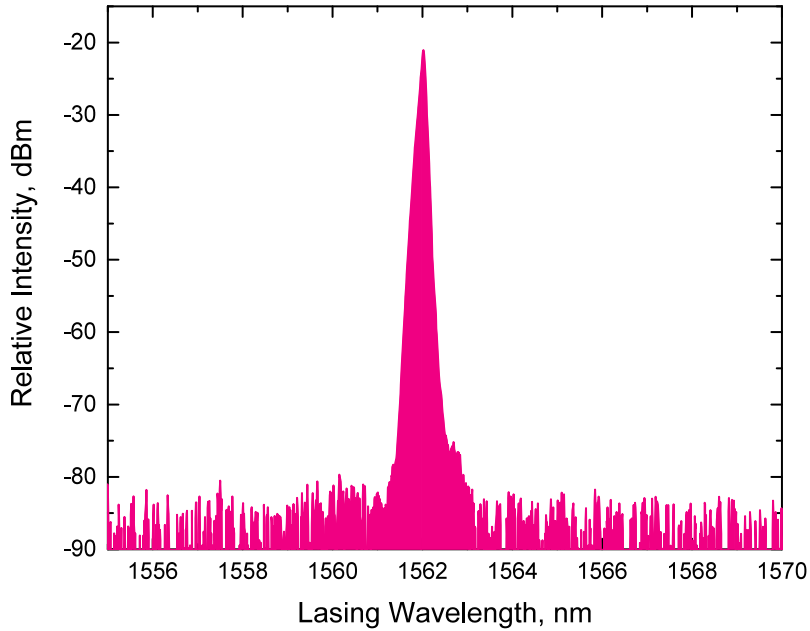


Figure 5.9: Lasing spectrum from MEMS VCSEL using 980 nm optical pumping on Setup1 (50X).

because of undesired change in focus of the microscope stage (due to the weight of the NIR camera).

### 5.3.2 Linewidth

The linewidth of the lasing spectrum for 980 nm pump laser was a little broad (Figure 5.9). A possible explanation for this is the thermal noise from heating up of Si MEMS by the 980 nm pump laser. The best way to test this hypothesis was to compare the laser spectra obtained for 980 nm and 1310 nm pumping. The spectrum obtained for 1310 nm pumping should be narrower due to the absence of any Si heating. Unfortunately, the power delivered by the 1310 nm using Setup1 was not enough for lasing. However, Setup2 avoids the lossy objectives. Thus, it was used to collect the lasing spectra from the same device using Setup2 but different pump sources. A very clear difference in the spectra FWHM can be observed (Figure 5.11). The FWHM is almost three times narrower with 1310 nm pumping. Furthermore, the FWHM measured for 1300 nm pumping

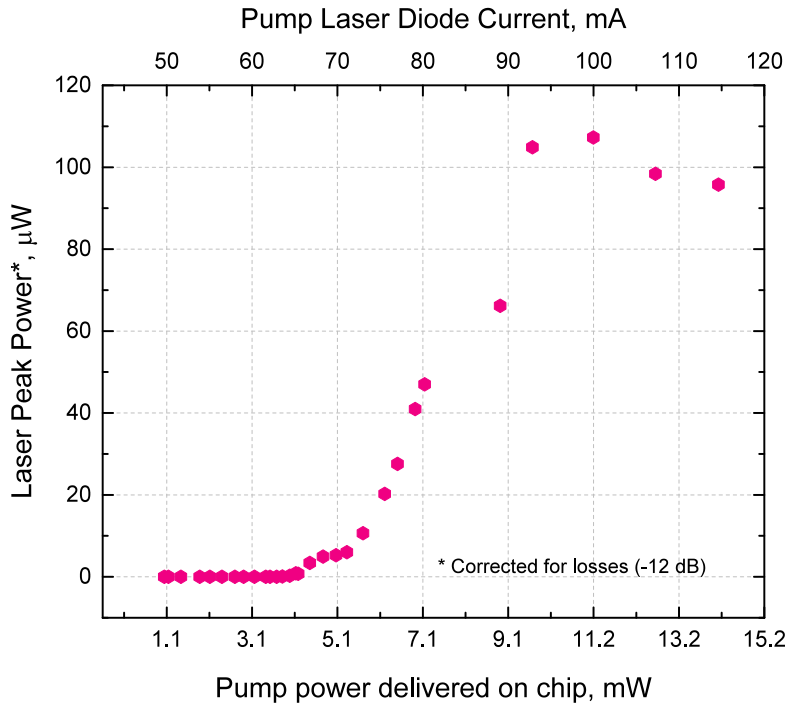


Figure 5.10: Laser peak power plotted against the pump power. The collected laser peak power is corrected for the losses in the system.



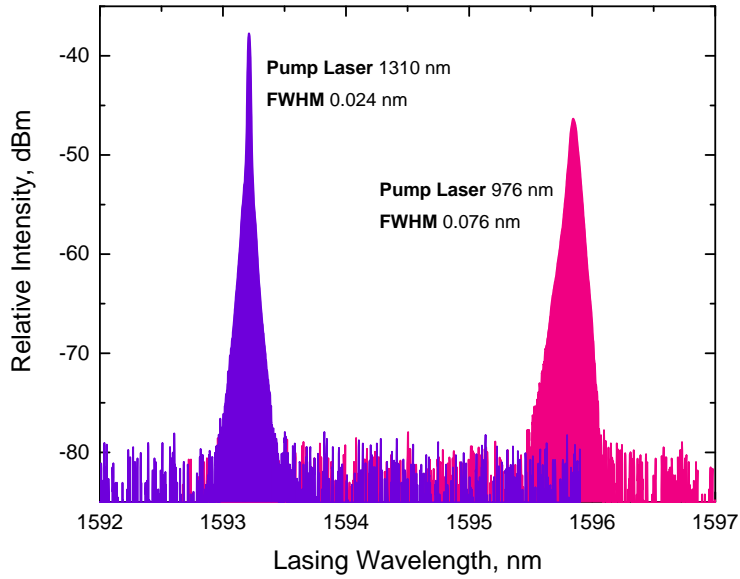


Figure 5.11: Lasing spectra obtained for 980 nm and 1310 nm pump laser using Setup2.

is close to the OSA measurement resolution of 0.01 nm. Thus it is same to conclude that the broad spectrum observed in the case of 980 nm pumping comes from heating in Si membrane and a very narrow linewidth of the lasing spectrum can be achieved for the fabricated MEMS VCSEL provided the 1310 nm pump laser was used.

It should be noted that a different sample was used for the linewidth experiment because of which the lasing wavelength differs from the earlier measurements. Also, between the two shown spectra, the one corresponding to 980nm pump has a slightly higher lasing wavelength most likely due to heating. The quantum defect<sup>3</sup> for a 980 nm laser is two times that of a 1310 nm laser.

<sup>3</sup> Quantum defect is the difference in energy between the absorbed and emitted photon.

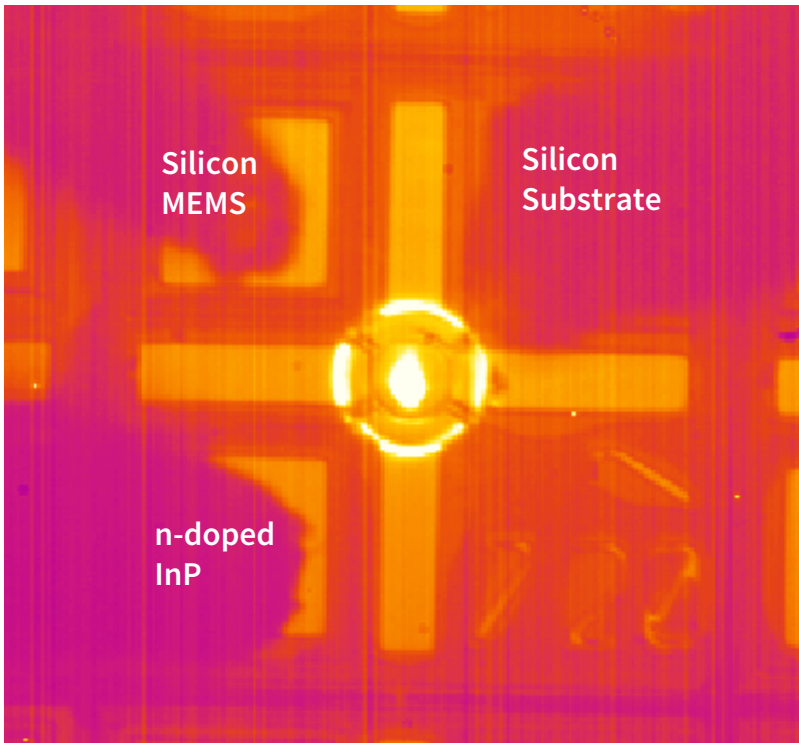


Figure 5.12: NIR image of the device showing lasing, with the three probes on the contact pads.

## 5.4 TUNING

The fabricated MEMS VCSEL, unlike existing MEMS VCSELs, uses three electrodes for actuation. The top electrode is defined by n-doped InP layer. The Si MEMS layer forms the centre electrode and the Si substrate constitutes the bottom electrode (Figure 5.12). Two types of tuning mechanisms were used for actuation- DC and AC. For DC actuation, a voltage was applied between the centre electrode and either of the other electrodes. The unused electrode was grounded. For AC actuation, voltage was applied only between Si MEMS and Si substrate.

#### 5.4.1 *DC Tuning*

Application of a voltage between the centre electrode and either top or bottom electrode creates an electrostatic attractive force between the two electrodes. This moves the mirror and changes the cavity length. As a result, we observe a change in the lasing wavelength. Figure 5.13 shows the change in lasing wavelength for different applied voltage. Application of a voltage between the Si MEMS and Si substrate increases the cavity length of VCSEL and we see laser tuning towards higher wavelength. A tuning range of around 40 nm was achieved. Similarly, a voltage between the Si MEMS and InP reduced the cavity length which moved the lasing curve to lower wavelength. Unfortunately, a wider tuning to lower wavelengths was not attained. The losses increased quite fast which restricted the tuning to just a couple of nm. Possible explanations include improper (not optimized) contacts or heating losses due to the short cavity or limitation from gain bandwidth. More investigation is required to trace the problem. Nevertheless, a total of 40 nm of DC tuning was achieved on the first generation fabricated MEMS VCSELs.

#### 5.4.2 *AC Tuning*

A combination of a sine wave and DC voltage was applied to look at the AC characteristics of the device. The voltage was applied between the Si MEMS layer and Si substrate. DC voltage has two contributions. First, it shifts the zero point of the AC signal. Second, the higher the DC voltage, the higher the electric field and more pronounced is the effect of AC signal.

Figure 5.14 shows a representative characteristic curve for an AC tuning. It is generally flat spectrum with characteristic peaks at both ends. It is because of the mechanical dynamics of the MEMS stage. For a mechanical oscillator, it is at zero velocity at the extreme ends, which leads to an increased collection time for the lasing signal and, thus, we see the characteristics curve with peaks at the ends. This curve only holds good when the tuning is done within the gain spectrum of the device. Else, the peaks disappear

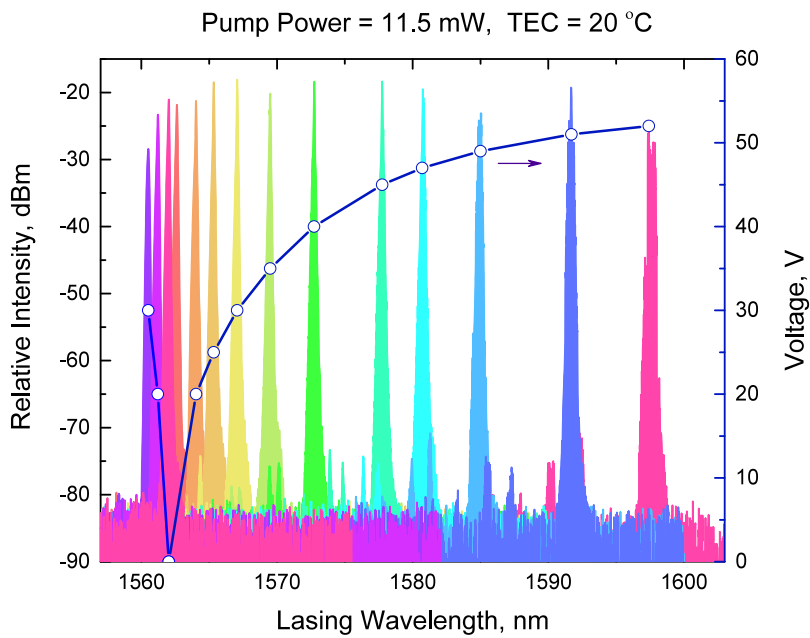


Figure 5.13: Lasing spectra showing wavelength tuning achieved for different actuation voltages. 980 nm laser diode was used for pumping.

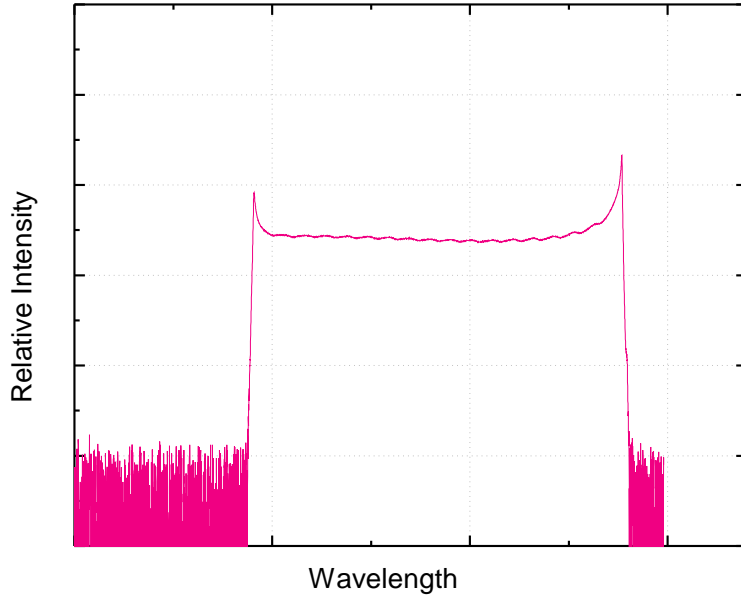


Figure 5.14: A representative AC tuning curve with the characteristics peaks at extreme ends.

as as seen in Figure 5.15. In this case <sup>4</sup>, the tuning range is not limited by the MEMS but by the active material. The tuning range achieved is far away from the expected range of close to 100 nm. The deviation can be either due to the unaccounted losses in the system or improper QW design.

The bandwidth of the AC spectrum is also dependent on the operating frequency. Operation close to the mechanical resonance increases the displacement and thus, increase the bandwidth (as shown in Figure 5.16). For the device in this discussion, the resonance frequency was obtained at 2.46 MHz. The resonance frequency response curve shown in 5.16, however, does not provide the accurate Q factor for the device. The bandwidth of the AC tuning curve was limited by gain material. Nevertheless, the peak around 2.4 MHz is a clear indication of the mechanical resonance of the MEMS stage.

<sup>4</sup> The device used for characterization in AC tuning is different from the one used for DC characterization.

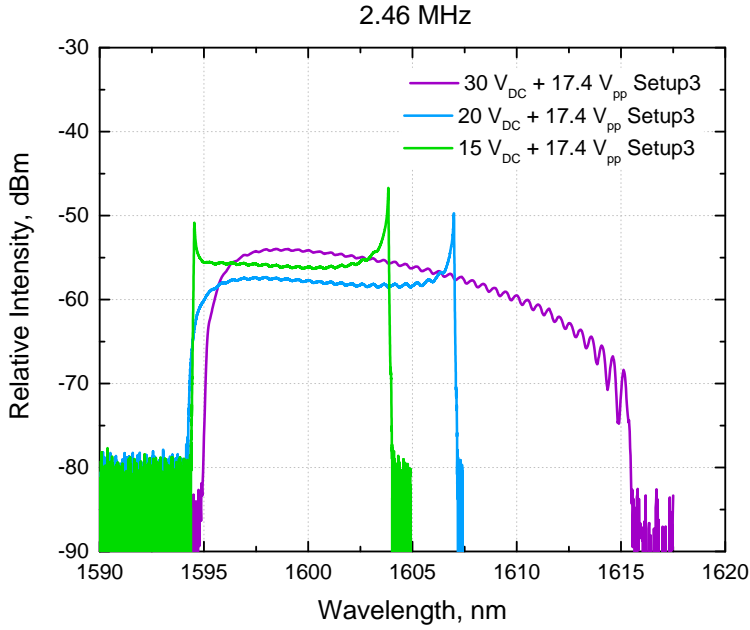


Figure 5.15: Lasing spectrum obtained for AC tuning.

#### 5.4.2.1 Resonance Frequency

The experimental resonance frequency for the MEMS VCSEL was 2.46 MHz, which is far from the simulated value - 0.88 MHz. As mentioned earlier, the simulation assumes vacuum around the MEMS stage and there is air inside the cavity. To be more specific, there are 2 cavities, one above and one below the MEMS. The closed cavity has a fixed volume with atmospheric pressure inside (Wafer bonding was done in air, RT). In addition, the design of the MEMS HCG (Figure 5.17) does not provide enough space for the air to exchange between the two cavities. When the mirror is moved under AC actuation, the air trapped in the top and bottom cavities act against the motion ( $PV = \text{constant}$ , under isothermal conditions). This translates to an increased stiffness of the spring system and thus an effective increase in the spring constant. So, the resonance frequency of the device can be controlled by constituents of the sealed cavity.

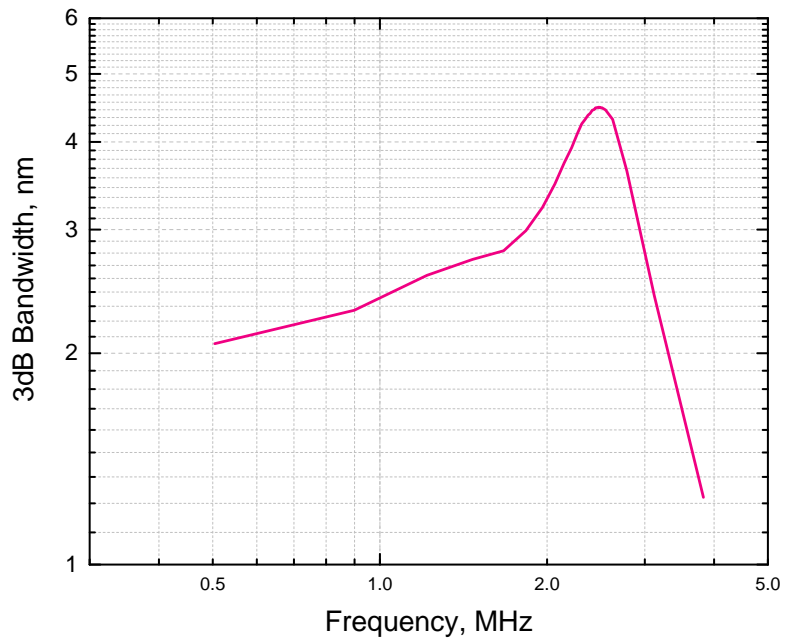


Figure 5.16: Resonance frequency response curve for the MEMS VCSEL. This does not give an accurate value of the Q factor of the device due to gain limited tuned bandwidth.

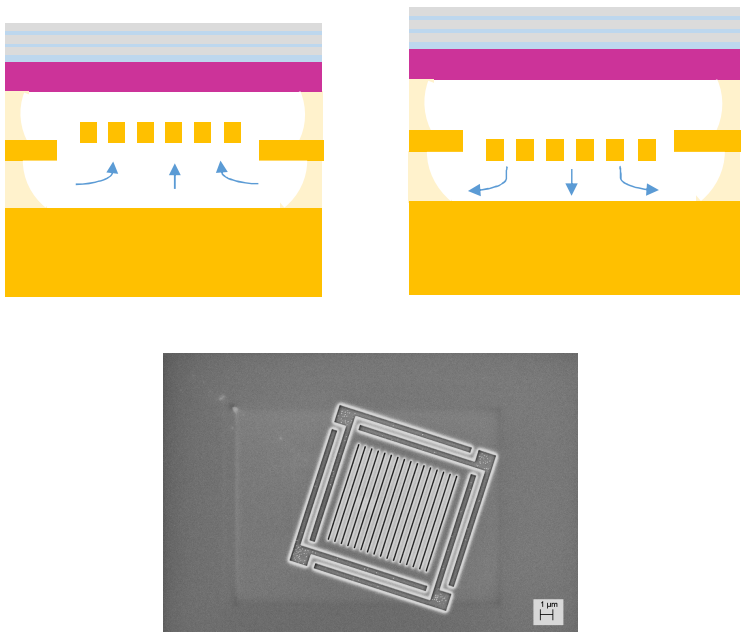


Figure 5.17: (Top) Illustration of the cavities present in the MEMS VCSEL and (bottom) a SEM top view of the device showing minimal access to the bottom cavity.



## 5.5 THERMAL EFFECT

Lasers are dependent on the operating temperature as it influences the gain spectrum, threshold carrier density, radiative/non-radiative recombination and overall refractive index of the system [63]. In addition, the device in discussion also relies on temperature for thermal lensing and, thus, lasing (Section 2.3.4). So, it was important to look at the effect of temperature on the laser. Apart from electrostatic actuation, the lasing wavelength is also controlled by the working temperature and pump power. There are two main sources of heat. First, when the device is optically pumped, the active region heats up locally primarily due to injected carriers. Second, any change in the substrate temperature also causes a shift. Figure 5.18 shows the shift in the peak of lasing wavelength for a change in substrate temperature and pumping power. At any given temperature, as the pumping power is increased, there is an increase in the generated carriers which increase the heat generated (non-radiative transitions) and thus contribute to the change in refractive index change. At a certain point, there will be carriers that do not contribute to the gain and only gives heat. Increasing the temperature of the substrate also contributes to the above mentioned effects. For moderate and low pumping powers, lasing wavelength has an almost linear dependence on temperature. However, the wavelength changes (increases) much more rapidly with the increase of pump power. On the other hand when the temperature of the substrate was varied, almost linear variation was observed for lower pumping values. The slope of the variation, however, increases with pump power. Pump power, being a local phenomenon, has a more profound effect than variations with the substrate temperature. The curve from Figure 5.18 can be used to estimate the amount of heating on the device. For example, for a 980 nm laser current of 69 mA, the device is heating at 38 °C, which is approx. 18 °C above room temperature.

## 5.6 ISSUES

The chip used for characterization was a 1-inch square SOI, bonded to a quarter of 2 inch InP wafer and each device occupied approximately 300  $\mu\text{m}$  x 300  $\mu\text{m}$ . So there were a lot of MEMS VCSELs on

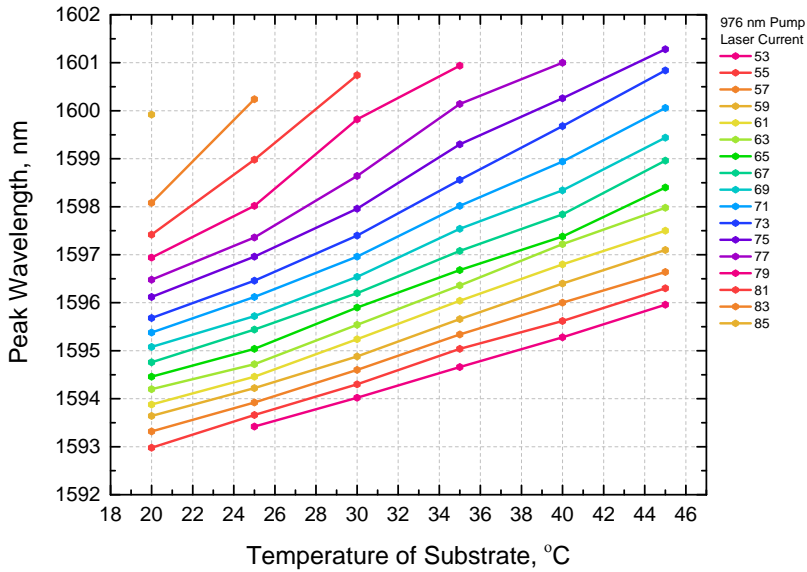


Figure 5.18: Shift in peak lasing wavelength of the MEMS VCSEL plotted against the substrate temperature for various pump laser power. 53 mA corresponds to the threshold for the MEMS VCSEL.

the chip. An illustration of the chip in reference to a quarter of 2-inch wafer is shown in Figure 5.19 with lasing wavelength of the device. Even though there were thousands of lasers on the chip, only around 80 were lasing and around 20 were tuning. As we argued earlier, the design brings in a lot of fabrication flexibility. So, the yield should have been much higher but unfortunately, it was too low.

To understand and identify the problem, focused ion beam (FIB) was done some of the devices. Figure 5.20 shows the SEM of the cross-section of a device. To our surprise, the buried oxide below the MEMS was not removed completely in most of the device. This had a direct influence on the HCG and MEMS and they did not perform as expected. The tuning range varied across the chip and some devices did not tune.

The unetched buried oxide was the result of decreased dry etch rate of spacer  $\text{SiO}_2$  (Section A.2). The etch process was developed on a 1-inch chip but a quarter of 6 inch SOI was used for the actual processing. Thus there was a huge change in load and this reduced

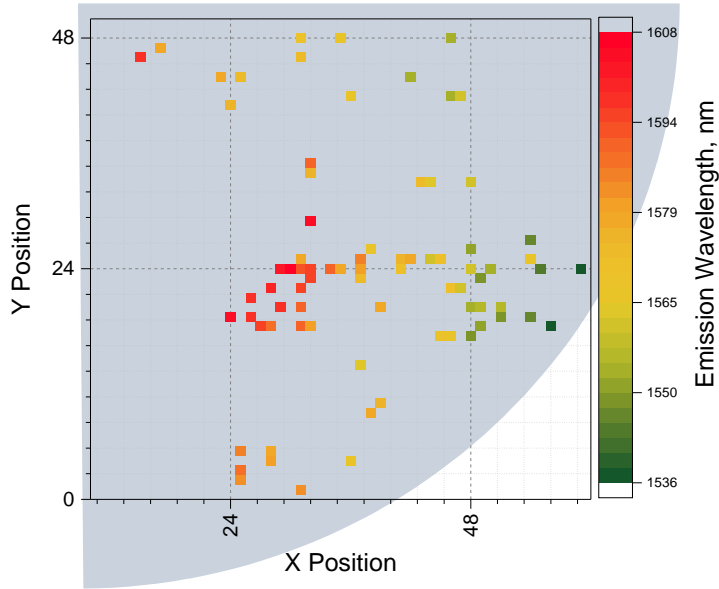


Figure 5.19: Illustration showing the location of lasing devices with their wavelength, on the characterized chip.

the dry etch rate resulting in incomplete etch of PBSG layer. Furthermore due to the slow etch rate of PBSG in bHF, thermal SiO<sub>2</sub> was hardly etched. Luckily, there was some non-uniformity in the dry etch, which resulted in some working devices. A future run with lessons from the current device and some optimization has definitely the promise to perform much better.

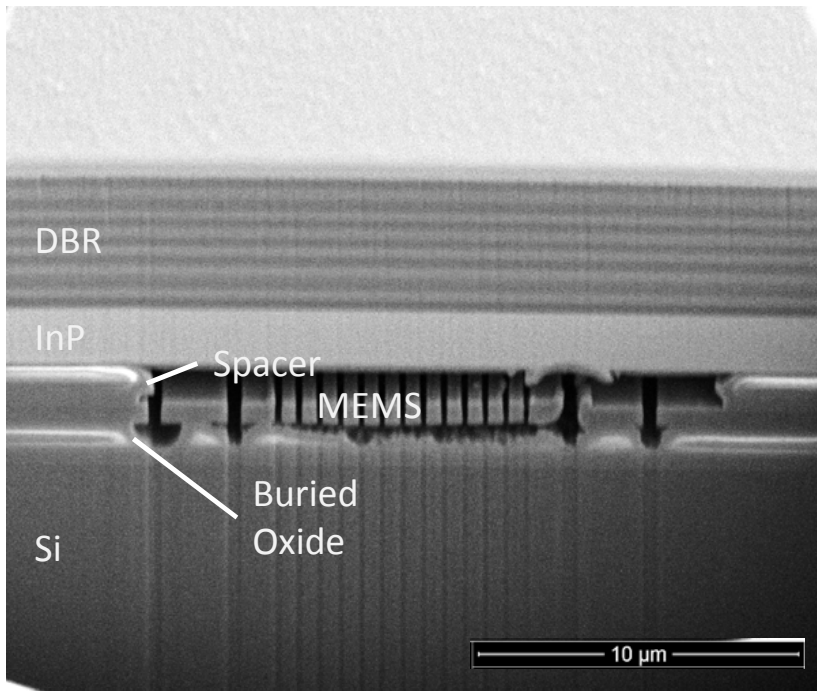


Figure 5.20: SEM image of FIB cross-section of the MEMSVCSEL showing an incomplete etch of the buried oxide below the MEMS structure.



## CONCLUSION AND OUTLOOK

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### 6.1 CONCLUSION

The primary aim of this thesis was to demonstrate a proof-of-concept device which was achieved. This work has studied and optimized the different elements forming the proposed MEMS VCSEL. An optimized process flow for fabricating the device has also been established. Lastly, the fabricated MEMS VCSEL was characterized by lasing and tuning parameters.

Theory and simulation of HCG mirror, dielectric DBR and device from previous experience [6] were built upon. In particular, the dielectric DBR mirrors were optimized after feedback from deposition done at DTU Danchip to have a high reflectivity at the emission wavelength and high transmission at the pump wavelengths. The thermal properties of the device were also studied. Heat pads were designed to extract heat efficiently from the VCSEL with a possibility to lower the core temperature by almost 30 °C. Thermal lensing, based on the heat profile from laser pumping, was simulated to look at the optical lasing modes. The MEMS stage for the HCG mirror was also simulated on COMSOL to find its mechanical resonance, which decides the maximum speed of operation of the MEMS VCSEL with the widest tuning range.

Fabrication of the designed MEMS VCSEL constituted the major task of the thesis. The proposed MEMS VCSEL moved away from the conventional design framework (III-V materials) to Si platform. So, the complete process flow for the device was designed as a part of this project. The enabling technology for the proposed device, integration of InP to patterned SOI wafers was also developed in this work. A systematic study was done to understand the bonding mechanism of hetero-material systems and a low temperature (300 °C) direct bonding method based on  $\text{Al}_2\text{O}_3$  as the intermediate material was presented. An interface energy as high as 1.7

J/m<sup>2</sup>(close to the theoretical maximum value) for Si-Si wafer bonding was achieved. The process was adapted to realize the proposed device. Still, the bonded wafers needed to have a clean surface free of particles and a surface roughness below 0.3 nm. So, all Si processing before bonding were optimized to have a bondable surface. Proper protocol for the handling of wafers before bonding was established to minimize particles and process flow was developed to achieve a SiO<sub>2</sub> bondable surface with roughness around 0.2 nm. Besides, Si and InP based deposition and etch processes were optimized to realize the device. Gold plating on the device to deposit thick metal heat pads was also explored and a protocol was established for deposition on future devices.

Finally, the fabricated device was characterized. Lasing with a low threshold corresponding to 1.4 mW was achieved, which is equivalent to 1 mA of electrical pumping. The lasing spectrum was narrow with a FWHM width of 0.024 nm, which is close to the OSA's measurement resolution of 0.01 nm. A wide DC tuning range of 40 nm was achieved with some degree of bi-directional tuning. AC actuation was also explored to find the resonance frequency of MEMS. A high-frequency operation of 2.4 MHz with a wide tuning range of around 15-20 nm was also achieved.

To conclude, this thesis has successfully proposed and realized a novel MEMS VCSEL which moves away from a III-V design framework to an established Si-platform. In doing so, the proposed device brings in a higher degree of robustness to the design. The proposed design has the potential to become the perfect SS of the future OCT systems.

## 6.2 OUTLOOK

The work presented in this thesis has a main focus on process development and establishment of fabrication process flow to realize the proposed MEMS VCSEL, which takes time. Within the short span of the project, only the first version of the device was fabricated and characterized. So, there is room for tweaking/optimizing the device to achieve state-of-art performance.

First, there are small changes which need to be done in the next run. The contact pads in the presented device were not optimized

to achieve ohmic contacts with all the layer as the metal stack used in this work was deposited using one mask. So, dedicated masks along with the appropriate metal stack should be used for contact definition. This should address the inability to tune wavelength in both directions. In addition, the dry etching time of  $\text{SiO}_2$  spacer layer before MEMS release (Section 5.6 and 4.1.3.2) must be corrected for a successful release of the MEMS HCG structure. The etch time used in the presented work was not sufficient due to an overlooked loading effect. The size of the wafer used for the actual run was much bigger than the one used for optimization. Addressing this issue should increase the fabrication yield many times.

Second, the proposed device can be improved upon on some fronts. The presented device was shown to be limited in the achieved tuning range by the gain spectrum. So, it can be addressed by the growth of better active material with wider gain and higher uniformity across the wafer. A wide gain can be achieved by the growth of multiple QW structures spread across the spectrum. Uniformity on a wafer scale, on the other hand, might be a bigger challenge to achieve as it is linked to the placement of wafers inside the growth chamber. Next, the MEMS HCG can be modified to also define the lasing mode. The current HCG defined on a MEMS stage is a set of parallel slits defined over a square region. Instead, the desired HCG can be defined in a circular fashion closely resembling the desired optical mode. Finally, tunnel junctions can be integrated with the proposed device to realize an electrically pumped MEMS VCSEL.

This thesis has realized a proof-of-concept for the proposed device and thus laid the foundation for future high performing MEMS VCSELS.





## Part IV

## APPENDIX



## FABRICATION PROCESS FLOW

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This chapter provides a detailed fabrication process flow used for the presented device. It can be used as a reference to fabricate MEMS VCSELs for any desired wavelength.

### A.1 WAFERS

SOI wafer was required to define the substrate and the bottom mirror. InP wafer was required to define the active material (QWs). Both were processed independently and bonded later on. The SOI wafer was custom ordered from IQE Silicon to have the desired device layer with required doping. The specifications are mentioned in Table A.1. The InP was grown in metalorganic vapour phase epitaxy (MOCVD) chamber at DTU Danchip. The information on the epitaxy layers is in Table A.3.

IQE SOI Wafer Spec Sheet	
Device layer thickness	$400 \pm 5$ nm
Device layer resistivity	n-type; $0.097 \Omega\text{cm}$
Box layer thickness	$1 \mu\text{m} \pm 5 \%$
Handle wafer resistivity	p-type; $1\text{-}5 \Omega\text{cm}$
Handle wafer thickness	$650 \pm 50 \mu\text{m}$
Wafer diameter	6 inch

Table A.1: Specification details of the SOI wafer used in the fabrication process

InP Substrate : $350 \pm 25 \mu\text{m}$		
Material	Thickness, nm	Comments
InP	164	Buffer
InGaAs	274	Stop layer for substrate etch
InP	105	
InAlAs	10	Barrier
InGaAlAs	15	
InGaAsP	7	QW in Barrier   Repeated 8 times
InGaAlAs	15	
InAlAs	10	Barrier
InP:Si	28	n++-doped InP layer for contact
InP:Si	1003	Bonding Interface layer
InGaAs:Si	24	Cap layers (Removed before bonding)
InP:Si	21	

Table A.3: Epitaxy growth sheet showing the approximate thickness of each layer. The growth starts on an InP wafer from the top of the table.

## A.2 SOI WAFER RCA CLEANING

The cap layers grown on the top of the InP wafer ensured cleanliness and were removed right before bonding. The SOI wafers on the other hand needed to be cleaned before any processing. An additional Piranha ( $4 \text{ H}_2\text{SO}_4$  (98%) :  $1 \text{ H}_2\text{O}_2$  (30%) ) could also be added before the RCA cleaning step.

Cleaning Process	
RCA 1	5 H <sub>2</sub> O : 1 NH <sub>4</sub> OH (25-29 %) : 1 H <sub>2</sub> O <sub>2</sub> (30 %)
RCA 2	5 H <sub>2</sub> O : 1 HCl (37 %) : 1 H <sub>2</sub> O <sub>2</sub> (30 %)
Temperature	70-80 °C
Time	10 min in each bath
5 % HF	
Temperature	Room Temperature
Time	30 sec

Table A.4: RCA Cleaning Process for Si wafers. A 30 sec HF dip after each RCA was performed to remove oxide formed during the cleaning process.

### A.3 E-BEAM PATTERNING

The mask for the bottom mirror was defined on e-beam using CSAR resist mask.

E-beam Resist Spin Recipe	
Resist	AR-P 6200/09 [5]
Speed	3500 rpm
Softbake	180 °C, 60 sec
Thickness	220 nm

Table A.5: Resist spin recipe for e-beam patterning. HMDS baking is not recommended for the resist. A thick layer of resist was chosen so as to survive the dry etch in the next step.

E-beam Exposure		E-beam Development	
Chuck	6 inch	Developer	AR 600-546
Dosage	300 $\mu$ C	Time	120 sec
Current Aperture	6 nA	Rinse	IPA, 60 sec

Table A.6: E-beam exposure (on JEOL JBX-9500FSZ at Danchip) and development. A longer development was essential to ensure complete development.

#### A.4 SILICON RIE ETCH ON PEGASUS

The following recipe was used for etching Silicon with CSAR mask. An Oxygen plasma cleaning of the chamber was performed at -20 °C before the etching step.

Recipe: nano1.42	
Gas (sccm)	C <sub>4</sub> F <sub>8</sub> (75), SF <sub>6</sub> (38)
Pressure	4 mTorr, Strike 3 secs @ 15 mTorr
Power	800 W CP, 40 W PP
Temperature	-20 °C
Etch Rate	~100 nm/min (For a 6 inch load)

Table A.7: Silicon etch recipe on Pegasus (DRIE System at Danchip) for etching HCG mirror. The recipe was developed by DTU Danchip. Care should be taken about the loading effect to get a better idea on the etch rate. For 4 inch wafer, the etch rate is around 160 nm/min.

At this point, the wafer was cleaved into 4 quarters and just one quarter was processed from here on. The etched wafer was then plasma ashed in oxygen for 20 min followed by RCA Cleaning (Table A.4). The cleaning was also essential in order to avoid contamination in the PECVD and annealing furnace chambers.

#### A.5 SPACER DEFINITION

The spacer layer was defined using two materials - SiO<sub>2</sub> and PBSG. This was done to achieve a small surface roughness by reflowing PBSG.

Recipe for SiO <sub>2</sub> Deposition	
Gas (sccm)	SiH <sub>4</sub> (17), N <sub>2</sub> O (1600)
Pressure	900 mTorr
Power	30 W (HF 13.56 MHz)
Electrode Temperature	250 °C (Top), 300 °C (Bottom)
Deposition Rate	~ 63 nm/min

Table A.8: High Frequency deposition recipe for SiO<sub>2</sub> on PECVD.

Recipe for PBSG Deposition	
Gas (sccm)	SiH <sub>4</sub> (17), N <sub>2</sub> O (1600), B <sub>2</sub> H <sub>6</sub> (135), PH <sub>3</sub> (40)
Pressure	900 mTorr
Power	800 W (LF 380 kHz)
Electrode Temperature	250 °C (Top), 300 °C (Bottom)
Deposition Rate	~ 209 nm/min

Table A.9: High Frequency deposition recipe for SiO<sub>2</sub>. The deposition rate was measured after annealing the test sample at 1000 °C.

PBSGfilm is highly hydrophobic. So, the sample was transferred immediately from PECVD chamber to anneal furnace chamber, where it was annealed in N<sub>2</sub> at 1000 °C for 40 min. The achieved surface roughness was 0.2 nm.

## A.6 SPACER ETCH AND CPD

A resist mask was used to define the opening on top of the MEMS, which defined the tunable air gap between the MEMS and the would be bonded InP layer.



AZ Resist Spin Recipe	
Preparation	HMDS Oven bake, 150°C, 15 min
Resist	AZ 5214E
Speed	2000 rpm - 2 steps
Softbake	90 °C, 90 sec
Thickness	2 $\mu\text{m}$

Table A.10: Resist spin recipe for AZ 5214E.

UV Exposure   365 nm (i-line)		UV Development	
Intensity	13 mW/cm <sup>2</sup>	Developer	AZ 726 MIF [9]
Dosage	130 mJ (10 sec)	Time	120 sec
Contact	Hard	Rinse	DIW, 5 min

Table A.11: Lithography parameters for exposure on Aligner (MA6 -2) and development on TMAH developer.

As mentioned in the Chapter 4, the spacer layer was etched using a 2 step process - ICP dry etch + bHF wet etch.

Recipe: sio_res	
Gas (sccm)	C <sub>4</sub> F <sub>8</sub> (5), H <sub>2</sub> (4)
Pressure	4 mTorr
Power	1300 W (Coil), 200 W (Platen)
Platen Temperature	20 °C
Etch Rate	~ 250 nm/min (4 inch load)
Etch depth	~ 700 nm (Spacer thickness 930 nm)

Table A.12: Etch recipe for SiO<sub>2</sub> on ICP (referred as AOE at Danchip) Etch using resist mask. Resist heats up from ion bombardment. Furthermore, the heat transfer is bad on a SOI wafer due to the presence of an oxide layer. So, the etch was done in steps of 20 sec. Care should be taken about loading. Etch rates will change a lot if the substrate is changed from a 4 inch to 6 inch.

The sample was then moved to a wet bench where the second part of the etch process was completed. The sample being in a

non-standard size, the following transfer process was followed in order to etch the buried oxide and release the MEMS safely. First the remaining spacer layer and the buried oxide is etched to release the MEMS. Then it is transferred to IPA before moving it into the CPD chamber

1. SiO Etch (bHF with surfactant) was used as the chemical for etch. The chemical was poured into a beaker and the wafer was dipped into the chemical. The time was calculated based on the oxide left to etch and the etch rates (Table A.13). The sample in the thesis was over etched by 5 min (~325 nm).
2. Once, the etch was complete, the acid was slowly removed from the beaker using an acid suction pipe while taking care that the sample was submerged at all times.
3. Carefully water was poured in to dilute and part of it was removed as mentioned in the previous step. This was repeated for 7-8 times so as to ensure almost all of the acid was removed. When using a water gun, special care was taken to avoid bubbles over the sample.
4. Using the acid suction pipe, water was removed until the point that the sample was still submerged. Ethanol was added until the top.
5. Ethanol was poured into another beaker and sample was transferred to this beaker quickly. The sample was held parallel to the surface, so that it held a liquid interface on top of it. This was impossible to do taking out of water as the surface was highly hydrophobic right after the bHF etch.
6. In a similar fashion, the sample was transferred into acetone.
7. The resist was removed in acetone. It took around 30 min for complete stripping of resist. During this process, the sample was kept vertical to ensure that resist did not fall back into the openings.
8. The sample was moved again for another acetone bath for 10 min.
9. Next, the sample was moved to IPA solution for 15 min.

Approximate Etch Rates ( nm/min)	
PECVD PBSG (reflow)	45
PECVD SiO <sub>2</sub>	145
Thermal SiO <sub>2</sub>	65

Table A.13: Etch rates for oxides in SiO Etch (bHF with surfactants). These should be considered as an indicative. The actual etch rate will depend on the etch openings.

10. The sample was then placed in IPA for 60 min, as a requirement from the CPD processing.
11. After that, the CPD chamber was opened and filled with required amount of IPA. The sample was then transferred from the IPA beaker to the chamber quickly.
12. CPD then took care of the release step using liquid CO<sub>2</sub>.

### A.7 BONDING

The InP wafer with QW structures (Table A.3) was also prepared for the bonding step by removal of the cap layers. The cap layers were etched in the following sequence - InP Etch , InGaAs Etch.

InP Etch (Diluted)	
Chemical	1 HCl (37 %) : 4 H <sub>3</sub> PO <sub>4</sub> (85 %)
Etch Rate	~ 500 nm/min
Temperature	RT
Etch Stop	InGaAs
Etch Time	30 sec

Table A.14: Recipe for etching InP cap layer.

InGaAs Etch	
Chemical	10 H <sub>2</sub> SO <sub>4</sub> (10 %) : 8 H <sub>2</sub> O <sub>2</sub> (30 %) : 71 H <sub>2</sub> O
Etch Rate	~ 500 nm/min
Temperature	RT
Etch Stop	InP
Etch Time	30 sec

Table A.15: Recipe for etching InP cap layer.

The InP wafer was rinsed with DIW and put into ALD chamber with the prepared SOI wafer from previous section. Approx. 2 nm of Al<sub>2</sub>O<sub>3</sub> was deposited on both wafers to help with the bonding.

ALD Al <sub>2</sub> O <sub>3</sub> Deposition		
Chemical	TMA	H <sub>2</sub> O
Nitrogen Flow	150 sccm	200 sccm
Pulse time	0.1 sec	0.1 sec
Purge time	3.0 sec	1.0 sec
Temperature	200 °C	
Number of cycles	25 cycles	
Deposition Rate	~ 1Å/cycle	

Table A.16: Recipe for depositing Al<sub>2</sub>O<sub>3</sub> using thermal ALD.

The wafers were bonded right after unloading from the chamber. The bonded sample was then annealed using a commercial wafer bonding system using the parameters listed in Table A.17.

Annealing Recipe: hikus_300C	
Temperature	300 °C
Chamber Pressure	3e-4mBar
Tool Pressure	1500 mBar
Duration	60 min

Table A.17: Recipe for depositing Al<sub>2</sub>O<sub>3</sub> using thermal ALD.

### A.8 SUBSTRATE ETCH

The InP substrate of the bonded sample was then etched away for further processing. But, first the thin layer of Al<sub>2</sub>O<sub>3</sub> deposited on the back of the InP wafer was etched away followed by the InP and InGaAs etch.

Recipe: hikus_Al2O3	
Gas (sccm)	BCl <sub>3</sub> (16), Cl <sub>2</sub> (4)
Pressure	2 mTorr
Coil Power	400 W
Platen Power	150 W
Platen Temperature	RT
Etch Rate	46 nm/min

Table A.18: Recipe for etching Al<sub>2</sub>O<sub>3</sub> on ICP (III-V ICP at Danchip).

InP Etch (Diluted)	
Chemical	HCl (37 %)
Etch Rate	~ 6 μm/min
Temperature	RT
Etch Stop	InGaAs

Table A.19: Recipe for etching InP cap layer.

The InP etch was monitored by measuring the thickness of the substrate every 15 min. It was followed by InGaAs etch (Table A.15). At this point, the sample was cleaved into 4 pieces (~ 1 inch side length) and etch to different layers was performed.

### A.9 ETCH TO N-DOPED INP LAYER

**MASK DEFINITION** The mask for the etch was defined using SiO<sub>2</sub> and a resist mask was used to define the SiO<sub>2</sub> mask. 100 nm SiO<sub>2</sub> was deposited on PECVD (Table A.8) and the resist mask was defined using the parameters listed in Table A.10 and A.11. Then,

bHF was used to transfer the mask to SiO<sub>2</sub> layer. This process of mask definition was also used in the next two sections.

InPwas etched in a combination of dry and wet etch steps. The layers etched were InP and QWs. The etch stop for the dry etch was QWs with Al content and the etch stop for the wet etch was the n-doped InP. RIE was used for dry etch (Table: A.20) and a mixture of sulfuric acid and peroxide was used for wet etch (Table A.21). The RIE process is a cyclic process with a etch step of 7 min followed by a oxygen plasma cleaning of 2 min.

Recipe: InPstd (RIE)	
Gas (sccm)	CH <sub>4</sub> (8.4), H <sub>2</sub> (42)
Pressure	80 mTorr
Power	60 W
Bias Voltage	450 V
Temperature	RT (Ion bombardment adds heat)
Etch Rate	29 nm/min (InP), 1 nm/min ( SiO <sub>2</sub> )

Table A.20: Recipe for dry etching InP on RIE. A chamber pre-conditioning was done before the etch.

QW Etch	
Chemical	1 H <sub>2</sub> SO <sub>4</sub> (10 %) : 1 H <sub>2</sub> O <sub>2</sub> (30 %)
Etch Rate	~ 1.7 μm/min
Temperature	RT
Etch Stop	n-doped InP

Table A.21: Recipe for wet etching QW layers.

The resist mask was stripped using oxygen plasma ashing and the SiO<sub>2</sub> mask was removed by bHF dip.

### A.10 ETCH TO SI MEMS LAYER

The mask for this etch was also defined similar to the previous section (A.9) The layers etched for this mask were InP, Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub>.

The InP layer was etched on RIE using Table A.20. Al<sub>2</sub>O<sub>3</sub> was etched on ICP using Table A.18 and SiO<sub>2</sub> was etched in a combination of dry (RIE - Table A.22) and wet etch (bHF). If the resist mask profile was damaged by ion-bombardment, the resist was stripped in oxygen plasma and the same mask was defined using lithography.

Recipe: SiO <sub>2</sub> _602 (RIE)	
Gas (sccm)	CHF <sub>3</sub> (16), O <sub>2</sub> (2)
Pressure	100 mTorr
Power	60 W
Bias Voltage	325 V
Temperature	RT (Ion bombardment adds heat)
Etch Rate	30 nm/min

Table A.22: Recipe for dry etching SiO<sub>2</sub> on RIE using a resist mask.

The dry etch was stopped with 200 nm of SiO<sub>2</sub> remaining. Then the resist mask was ashed away and the remaining oxide along with the oxide mask were removed together in bHF.

### A.11 ETCH TO SI SUBSTRATE

The mask for the last set of etches was also defined as described in A.9. The development time was increased by 120 sec to ensure complete development. The layer etched were Si and SiO<sub>2</sub>. Si was etched on ICP using the paramters given below (Table A.23) and SiO<sub>2</sub> was etched in a combination of dry (RIE - Table A.22) and wet etch (bHF), exactly as done in the previous section.

Recipe: Si Etch (III V ICP)	
Gas (sccm)	SF <sub>6</sub> (40), O <sub>2</sub> (27)
Pressure	80 mTorr
Platen Power	100 W
Coil Power	0
Temperature	20 °C
Etch Rate	450 nm/min

Table A.23: Recipe for dry etching Si on ICP using a resist mask. It is actually a RIE process done in a ICP chamber.

## A.12 CONTACT DEPOSITION

The mask for the contact depositions was also defined using a combination of SiO<sub>2</sub> and resist. There were few different considerations here though. SiO<sub>2</sub> deposited also served as the first layer of the DBR layer. So, the thickness of the SiO<sub>2</sub> layer was based on the desired DBR structure. And a negative resist was used here. The resist was patterned using Tables A.24, A.25 and then the SiO<sub>2</sub> mask was defined by bHF.

AZ nLOF 2070 Spin Recipe	
Preparation	HMDS Oven bake, 150 °C, 15 min
Resist	AZ nLOF 2070
Speed	3000 rpm- 60 sec - 3 steps
Softbake	110 °C, 90 sec
Thickness	7 μm
Post Exposure Bake	110 °C, 90 sec

Table A.24: Resist spin recipe for AZ nLOF 2070 patterning. The resist was allowed to settle down (60 sec) before spinning to ensure there were no bubbles trapped.



UV Exposure   365 nm (i-line)		UV Development	
Intensity	13 mW/cm <sup>2</sup>	Developer	AZ 726 MIF [9]
Dosage	195 mJ (15 sec)	Time	(120 + 60 + 30 + 30 ) sec
Contact	Hard	Rinse	DIW, 5 min

Table A.25: Lithography parameters for exposure on Aligner (MA6 -2) and development on TMAH developer for nLOF 2070.

The bHF etch was done right before the contact definition to ensure a clean deposition. The metal stack (25 nm Ti, 75 nm Pt and 300 nm Au) was then deposited using e-beam evaporation. The process was completed by a liftoff process in acetone.It took roughly 30 min to strip all the resist.

### A.13 DBR DEPOSITION

The top mirror deposition was made at Chalmers using a sputter deposition system. The mask was defined using nLOF resist with the parameters listed in Table A.24 and A.25. Since, the first layer was deposited in the previous section, the deposition started from the second layer. The individual layer thicknesses are mentioned in Table A.26.

DBR Composition	
TiO <sub>2</sub>	187 nm
SiO <sub>2</sub>	234 nm
TiO <sub>2</sub>	206 nm
SiO <sub>2</sub>	320 nm
TiO <sub>2</sub>	143 nm
SiO <sub>2</sub>	227 nm
TiO <sub>2</sub>	191 nm
SiO <sub>2</sub>	244 nm
TiO <sub>2</sub>	146 nm
SiO <sub>2</sub>	274 nm
TiO <sub>2</sub>	153 nm
SiO <sub>2</sub>	365 nm
TiO <sub>2</sub>	152 nm
SiO <sub>2</sub>	304 nm
InP bonded to SOI	

Table A.26: The deposited DBR stack with individual layer thicknesses.

Post deposition, the liftoff was done using Microposit Remover 1165 at 60 °C for 15-20 min.

## A.14 CONTACT DEFINITION WITH THICK AU

Thermal simulation in chapter 2 showed placement and thickness of Au was critical for efficient heat transfer from the center of VCSEL (Refer heating pad design). However, a maximum of 300 nm of Au was allowed on the deposition tool. So, an alternate process flow was also designed for the device run where heat transfer would be critical.

The thick Au layer was achieved using Au plating. The following steps should be inserted between the Contact Deposition (A.12) and DBR Deposition (A.13).

1. A blanket deposition of 1 nm Ti, 50 nm Au, 5 nm Ti was done on all over the sample. This was the seed layer for the Au

plating. The top Ti was to increase the adhesion with the resist mask. Ti in the open areas was etched away before plating (5 sec in bHF).

2. The mask for the plating was defined using the following parameters.

AZ 15nXT Spin Recipe	
Preparation	HMDS Oven bake, 150 °C, 15 min
Resist	AZ 15nXT [77]
Speed	6000 rpm- 60 sec - 2 steps
Softbake	110 °C, 300 sec
Thickness	4-5 $\mu\text{m}$
Post Exposure Bake	120 °C, 60 sec

Table A.27: Resist spin recipe for AZ 15nXT patterning. The resist was designed for electroplating.

UV Exposure   365 nm (i-line)		UV Development	
Intensity	13 mW/cm <sup>2</sup>	Developer	AZ 726 MIF [9]
Dosage	250 mJ (19.5 sec)	Time	(120 + 60 ) sec
Contact	Hard	Rinse	DIW, 5 min

Table A.28: Lithography parameters for exposure on Aligner (MA6 -2) and development on TMAH developer for AZ 15nXT.

3. The sample was then Au plated by our collaborators at IPU. The expected thickness was achieved by correctly measuring the area of deposition and then adjusting the plating parameters.
4. The resist mask then removed using Microposit Remover 1165 at 50 °C.
5. Finally the 5nm Ti and 50 nm Au blanket layers were removed using bHF and potassium iodide (KI) etch respectively.

## A.15 DBR DEPOSITION USING IBSD

As per the initial plan, DBR deposition was planned to be done using ion assisted sputter deposition system. The process was developed on ion beam sputter deposition (IBSD) but could not be used for the real sample. The following process flow was developed for a mirror deposition on IBSD

1. The sputter system was calibrated to have the correct tooling factor for both  $\text{SiO}_2$  and  $\text{TiO}_2$ . This was done by depositing 50 nm of each using their old tooling factors followed by measurement of actual deposition thickness. The tooling factor was then found by  $\text{Tooling}_{Actual} = \frac{\text{Tooling}_{Used} \times \text{Thickness}_{Actual}}{\text{Thickness}_{Used}}$
2. The mask was defined in the same way as done in A.13.
3. Taking into considerations the refractive index information from deposition done in step 1, the individual layer thicknesses were determined.
4. The optimized dielectric stack was then deposited followed by liftoff in Microposit Remover 1165.



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